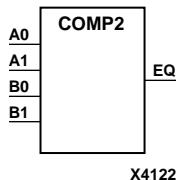


COMP2, 4, 8, 16

2-, 4-, 8-, 16-Bit Identity Comparators

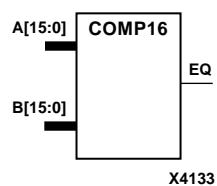
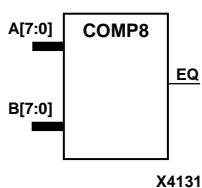
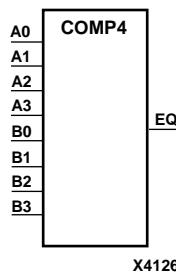
Architectures Supported

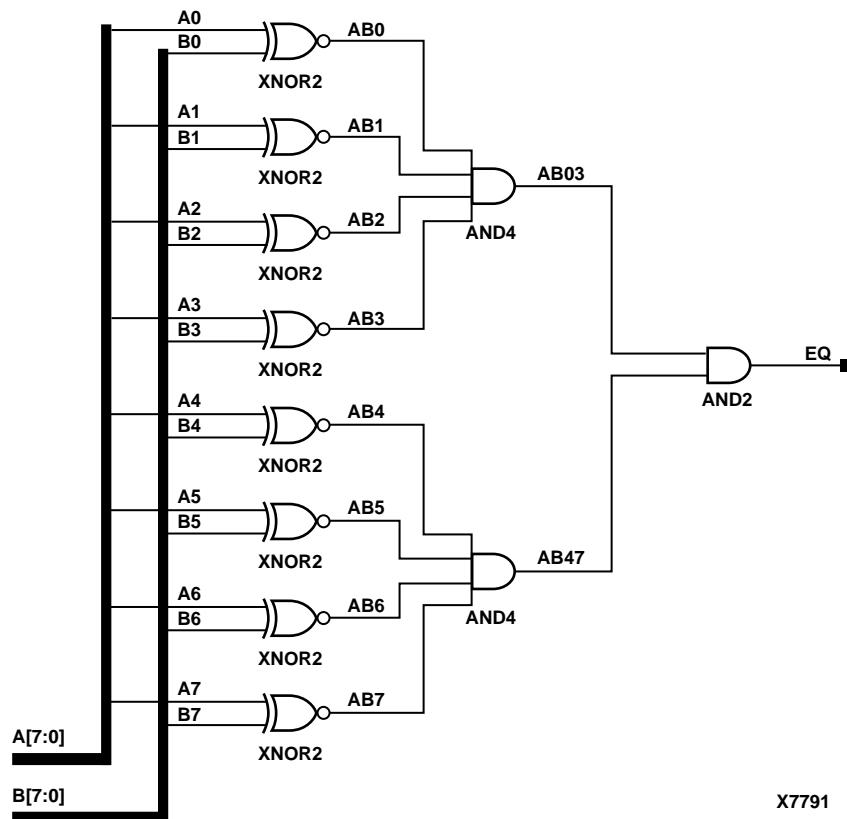
COMP2, COMP4, COMP8, COMP16	
Spartan-II, Spartan-IIIE	Macro
Spartan-3	Macro
Virtex, Virtex-E	Macro
Virtex-II, Virtex-II Pro, Virtex-II Pro X	Macro
XC9500, XC9500XV, XC9500XL	Macro
CoolRunner XPLA3	Macro
CoolRunner-II	Macro
CoolRunner-IIS	No



COMP2, COMP4, COMP8, and COMP16 are, respectively, 2-, 4-, 8-, and 16-bit identity comparators. The equal output (EQ) of the COMP2 2-bit, identity comparator is High when the two words A1 – A0 and B1 – B0 are equal. EQ is high for COMP4 when A3 – A0 and B3 – B0 are equal; for COMP8, when A7 – A0 and B7 – B0 are equal; and for COMP16, when A15 – A0 and B15 – B0 are equal.

Equality is determined by a bit comparison of the two words. When any two of the corresponding bits from each word are not the same, the EQ output is Low.





COMP8 Implementation XC9500/XV/XL, CoolRunner XPLA3, CoolRunner-II, Spartan-II, Spartan-IIIE, Spartan-3, Virtex, Virtex-E, Virtex-II, Virtex-II Pro, Virtex-II Pro X

Usage

For HDL, these design elements are inferred rather than instantiated.

VHDL Inference Code

```
architecture behavioral of comp2 is
```

```

begin
  process (A, B)
  begin
    If (A=B) then
      EQ <= '1';
    else
      EQ <= '0';
    end if;
  end process;
end behavioral;
```

Verilog Inference Code

```
always @ (A or B)
begin
  if (A == B)
    EQ <= 1;
  else
    EQ <= 0;
end
```

