

GND

Ground-Connection Signal Tag

Architectures Supported

GND	
Spartan-II, Spartan-IIE	Primitive
Spartan-3	Primitive
Virtex, Virtex-E	Primitive
Virtex-II, Virtex-II Pro, Virtex-II Pro X	Primitive
XC9500, XC9500XV, XC9500XL	Primitive
CoolRunner XPLA3	Primitive
CoolRunner-II	Primitive
CoolRunner-IIS	No



X3858

The GND signal tag, or parameter, forces a net or input function to a Low logic level. A net tied to GND cannot have any other source.

When the logic-trimming software or fitter encounters a net or input function tied to GND, it removes any logic that is disabled by the GND signal. The GND signal is only implemented when the disabled logic cannot be removed.

Usage

For HDL, this design element can be instantiated or inferred.

VHDL Inference Code:

```
gnd_signal <= '0';
```

Verilog Inference Code:

```
assign gnd_signal = 0;
```

VHDL Instantiation Template

```
-- Component Declaration for GND should be placed
-- after architecture statement but before begin keyword

component GND
  port (G : out STD_ULOGIC);
end component;

-- Component Attribute specification for GND
-- should be placed after architecture declaration but
-- before the begin keyword

-- Enter constraints here

-- Component Instantiation for GND should be placed
-- in architecture after the begin keyword
```

```
GND_INSTANCE_NAME : GND
    port map (G => user_G);
```

Verilog Instantiation Template

```
GND GND_instance_name (.G (user_G));
```

Commonly Used Constraints

None