

VCC

VCC-Connection Signal Tag

Architectures Supported

VCC	
Spartan-II, Spartan-IIIE	Primitive
Spartan-3	Primitive
Virtex, Virtex-E	Primitive
Virtex-II, Virtex-II Pro, Virtex-II Pro X	Primitive
XC9500, XC9500XV, XC9500XL	Primitive
CoolRunner XPLA3	Primitive
CoolRunner-II	Primitive
CoolRunner-IIS	No

vcc
—
x8721

The VCC signal tag or parameter forces a net or input function to a logic High level. A net tied to VCC cannot have any other source.

When the placement and routing software encounters a net or input function tied to VCC, it removes any logic that is disabled by the VCC signal. The VCC signal is only implemented when the disabled logic cannot be removed.

Usage

For HDL, this design element can be instantiated or inferred.

VHDL Inference Code

```
vcc_signal <= '1';
```

Verilog Inference Code

```
assign vcc_signal = 1;
```

VHDL Instantiation Template

```
-- Component Declaration for VCC should be placed
-- after architecture statement but before begin keyword

component VCC
    port (P : out STD_ULOGIC);
end component;

-- Component Attribute specification for VCC
-- should be placed after architecture declaration but
-- before the begin keyword

-- Enter attributes here

-- Component Instantiation for VCC should be placed
-- in architecture after the begin keyword
```

```
VCC_INSTANCE_NAME : VCC
    port map (P => user_P);
```

Verilog Instantiation Template

```
VCC instance_name (.P (user_P));
```

Commonly Used Constraints

None