Spartan-IIE 1.8V FPGA Family: Introduction and Ordering Information

DS077-1 (v2.2) July 28, 2004

Product Specification

Introduction

The Spartan™-IIE 1.8V Field-Programmable Gate Array family gives users high performance, abundant logic resources, and a rich feature set, all at an exceptionally low price. The seven-member family offers densities ranging from 50,000 to 600,000 system gates, as shown in Table 1. System performance is supported beyond 200 MHz.

Spartan-IIE devices deliver more gates, I/Os, and features per dollar than other FPGAs by combining advanced process technology with a streamlined architecture based on the proven Virtex™-E platform. Features include block RAM (to 288K bits), distributed RAM (to 221,184 bits), 19 selectable I/O standards, and four DLLs (Delay-Locked Loops). Fast, predictable interconnect means that successive design iterations continue to meet timing requirements.

The Spartan-IIE family is a superior alternative to mask-programmed ASICs. The FPGA avoids the initial cost, lengthy development cycles, and inherent risk of conventional ASICs. Also, FPGA programmability permits design upgrades in the field with no hardware replacement necessary (impossible with ASICs).

Features

- Second generation ASIC replacement technology
  - Densities as high as 15,552 logic cells with up to 600,000 system gates
  - Streamlined features based on Virtex-E architecture
  - Unlimited in-system reprogrammability
  - Very low cost
  - Advanced 0.15 micron technology
- System level features
  - SelectRAM+™ hierarchical memory:
    - 16 bits/LUT distributed RAM
    - Configurable 4K-bit true dual-port block RAM
    - Fast interfaces to external RAM
  - Fully 3.3V PCI compliant to 64 bits at 66 MHz and CardBus compliant
  - Low-power segmented routing architecture
  - Dedicated carry logic for high-speed arithmetic
  - Efficient multiplier support
  - Cascade chain for wide-input functions
  - Abundant registers/latches with enable, set, reset
  - Four dedicated DLLs for advanced clock control
    - Eliminate clock distribution delay
    - Multiply, divide, or phase shift
  - Four primary low-skew global clock distribution nets
  - IEEE 1149.1 compatible boundary scan logic
- Versatile I/O and packaging
  - Pb-free package options
  - Low-cost packages available in all densities
  - Family footprint compatibility in common packages
  - 19 high-performance interface standards
    - LVTTL, LVCMOS, HSTL, SSTL, AGP, CTT, GTL
    - LVDS and LVPECL differential I/O
  - Up to 205 differential I/O pairs that can be input, output, or bidirectional
  - Hot swap I/O (CompactPCI friendly)
- Fully supported by powerful Xilinx ISE development system
  - Fully automatic mapping, placement, and routing
  - Integrated with design entry and verification tools
  - Extensive IP library including DSP functions and soft processors

Table 1: **Spartan-IIE FPGA Family Members**

Device	Logic Cells	Typical System Gate Range (Logic and RAM)	CLB Array (R x C)	Total CLBs	Maximum Available User I/O(1)	Maximum Differential I/O Pairs	Distributed RAM Bits	Block RAM Bits
XC2S50E	1,728	23,000 - 50,000	16 x 24	384	182	83	24,576	32K
XC2S100E	2,700	37,000 - 100,000	20 x 30	600	202	86	38,400	40K
XC2S150E	3,888	52,000 - 150,000	24 x 36	864	265	114	55,296	48K
XC2S200E	5,292	71,000 - 200,000	28 x 42	1,176	289	120	75,264	56K
XC2S300E	6,912	93,000 - 300,000	32 x 48	1,536	329	120	98,304	64K
XC2S400E	10,800	145,000 - 400,000	40 x 60	2,400	410	172	153,600	160K
XC2S600E	15,552	210,000 - 600,000	48 x 72	3,456	514	205	221,184	288K

Notes:

1. User I/O counts include the four global clock/user input pins. See details in Table 2, page 3

General Overview

The Spartan-IIE family of FPGAs have a regular, flexible, programmable architecture of Configurable Logic Blocks (CLBs), surrounded by a perimeter of programmable Input/Output Blocks (IOBs). There are four Delay-Locked Loops (DLLs), one at each corner of the die. Two columns of block RAM lie on opposite sides of the die, between the CLBs and the IOB columns. The XC2S400E has four columns and the XC2S600E has six columns of block RAM. These functional elements are interconnected by a powerful hierarchy of versatile routing channels (see Figure 1).

Spartan-IIE FPGAs are customized by loading configuration data into internal static memory cells. Unlimited reprogramming cycles are possible with this approach. Stored values in these cells determine logic functions and interconnections implemented in the FPGA. Configuration data can be read from an external serial PROM (master serial mode), or written into the FPGA in slave serial, slave parallel, or Boundary Scan modes. Xilinx offers multiple types of low-cost configuration solutions including the Platform Flash in-system programmable configuration PROMs.

Spartan-IIE FPGAs are typically used in high-volume applications where the versatility of a fast programmable solution adds benefits. Spartan-IIE FPGAs are ideal for shortening product development cycles while offering a cost-effective solution for high volume production.

Spartan-IIE FPGAs achieve high-performance, low-cost operation through advanced architecture and semiconductor technology. Spartan-IIE devices provide system clock rates beyond 200 MHz. In addition to the conventional benefits of high-volume programmable logic solutions, Spartan-IIE FPGAs also offer on-chip synchronous single-port and dual-port RAM (block and distributed form), DLL clock drivers, programmable set and reset on all flip-flops, fast carry logic, and many other features.

Spartan-IIE Family Compared to Spartan-II Family

- Higher density and more I/O
- Higher performance
- Unique pinouts in cost-effective packages
- Differential signaling
  - LVDS, Bus LVDS, LVPECL
- V_{CCINT} = 1.8V
  - Lower power
  - 5V tolerance with external resistor
  - 3V tolerance directly
- PCI, LVTTL, and LVCMOS2 input buffers powered by V_{CCO} instead of V_{CCINT}
- Unique larger bitstream

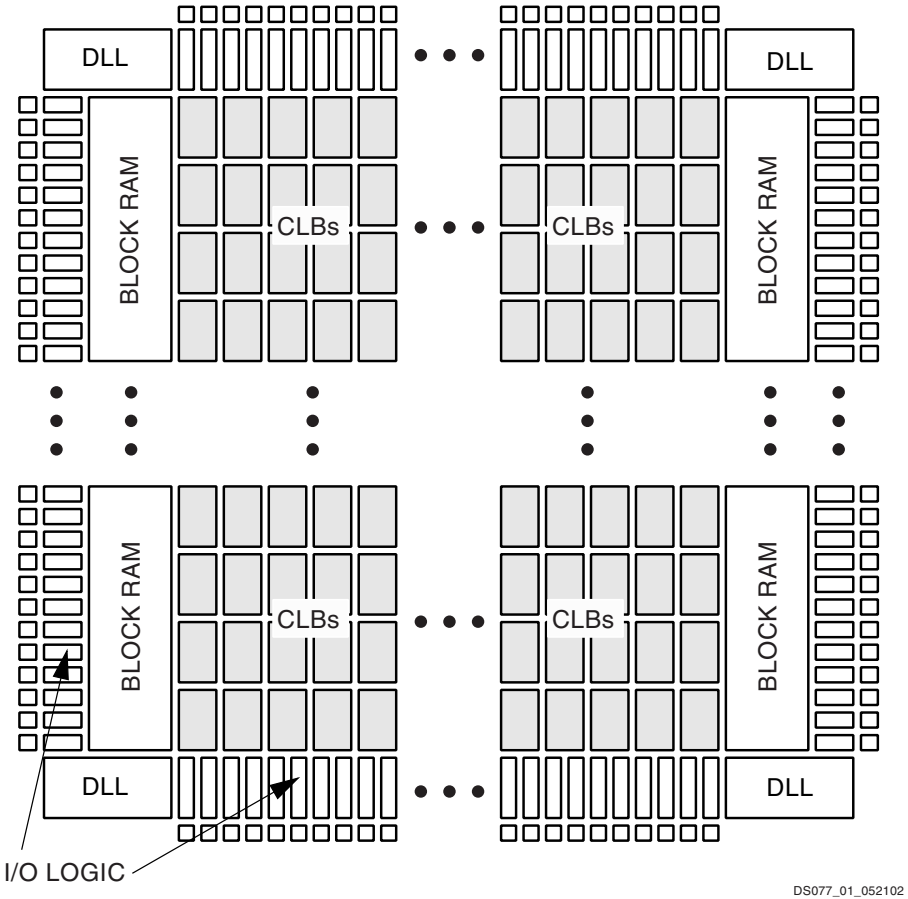


Figure 1: **Basic Spartan-IIE Family FPGA Block Diagram**

Spartan-IIE Product Availability

Table 2 shows the maximum user I/Os available on the device and the number of user I/Os available for each device/package combination.

Table 2: **Spartan-IIE User I/O Chart**

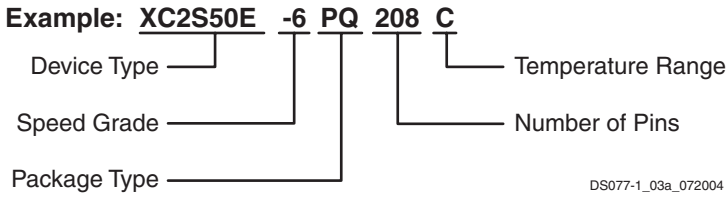
Device	Maximum User I/O	Available User I/O According to Package Type				
		TQ144 TQG144	PQ208 PQG208	FT256 FTG256	FG456 FGG456	FG676 FGG676
XC2S50E	182	102	146	182	-	-
XC2S100E	202	102	146	182	202	-
XC2S150E	265	-	146	182	265	-
XC2S200E	289	-	146	182	289	-
XC2S300E	329	-	146	182	329	-
XC2S400E	410	-	-	182	329	410
XC2S600E	514	-	-	-	329	514

Notes:
1. User I/O counts include the four global clock/user input pins.

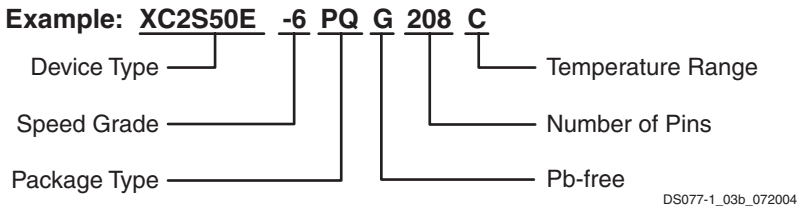
Ordering Information

Spartan-IIE devices are available in both standard and Pb-free packaging options for all device/package combinations. The Pb-free packages include a special "G" character in the ordering code.

Standard Packaging



Pb-Free Packaging



Device Ordering Options

Device
XC2S50E
XC2S100E
XC2S150E
XC2S200E
XC2S300E
XC2S400E
XC2S600E

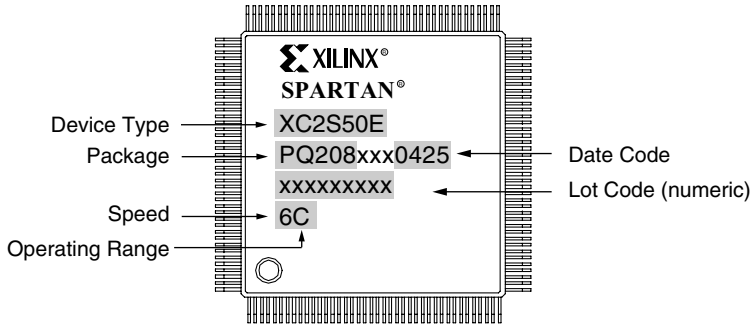
Speed Grade	
-6	Standard Performance
-7	Higher Performance[1]

Package Type / Number of Pins	
TQ(G)144	144-pin Plastic Thin QFP
PQ(G)208	208-pin Plastic QFP
FT(G)256	256-ball Fine Pitch BGA
FG(G)456	456-ball Fine Pitch BGA
FG(G)676	676-ball Fine Pitch BGA

Temperature Range (T_J)[2]	
C = Commercial	0°C to +85°C
I = Industrial	–40°C to +100°C

Notes:
1. The -7 speed grade is exclusively available in the Commercial temperature range.
2. See **www.xilinx.com** for information on automotive temperature range devices.

Device Part Marking



Sample package with part marking for XC2S50E-6PQ208C.

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The Spartan-IIE Family Data Sheet

DS077-1, ***Spartan-IIE 1.8V FPGA Family: Introduction and Ordering Information*** (Module 1)

DS077-2, ***Spartan-IIE 1.8V FPGA Family: Functional Description*** (Module 2)

DS077-3, ***Spartan-IIE 1.8V FPGA Family: DC and Switching Characteristics*** (Module 3)

DS077-4, ***Spartan-IIE 1.8V FPGA Family: Pinout Tables*** (Module 4)

Revision History

Date	Version No.	Description
06/27/02	1.1	Updated -7 availability.
11/18/02	2.0	Added XC2S400E and XC2S600E. Corrected XC2S150E max I/O count and XC2S50E differential I/O count and updated availability.
07/09/03	2.1	Noted hot-swap capability. Updated Table 2 to show that all products are available. Clarified device part marking.
07/28/04	2.2	Added information on Pb-free packaging options.

Spartan-IIE 1.8V FPGA Family: Functional Description

DS077-2 (v2.1) July 9, 2003

Product Specification

Architectural Description

Spartan-IIE Array

The Spartan-IIE user-programmable gate array, shown in Figure 1, is composed of five major configurable elements:

- IOBs provide the interface between the package pins and the internal logic
- CLBs provide the functional elements for constructing most logic
- Dedicated block RAM memories of 4096 bits each
- Clock DLLs for clock-distribution delay compensation and clock domain control
- Versatile multi-level interconnect structure

As can be seen in Figure 1, the CLBs form the central logic structure with easy access to all support and routing structures. The IOBs are located around all the logic and memory elements for easy and quick routing of signals on and off the chip.

Values stored in static memory cells control all the configurable logic elements and interconnect resources. These values load into the memory cells on power-up, and can reload if necessary to change the function of the device.

Each of these elements will be discussed in detail in the following sections.

Input/Output Block

The Spartan-IIE IOB, as seen in Figure 2, features inputs and outputs that support a wide variety of I/O signaling standards. These high-speed inputs and outputs are capable of supporting various state of the art memory and bus interfaces. Table 1 lists several of the standards which are supported along with the required reference, output and termination voltages needed to meet the standard.

The three IOB registers function either as edge-triggered D-type flip-flops or as level-sensitive latches. Each IOB has a clock signal (CLK) shared by the three registers and independent Clock Enable (CE) signals for each register.

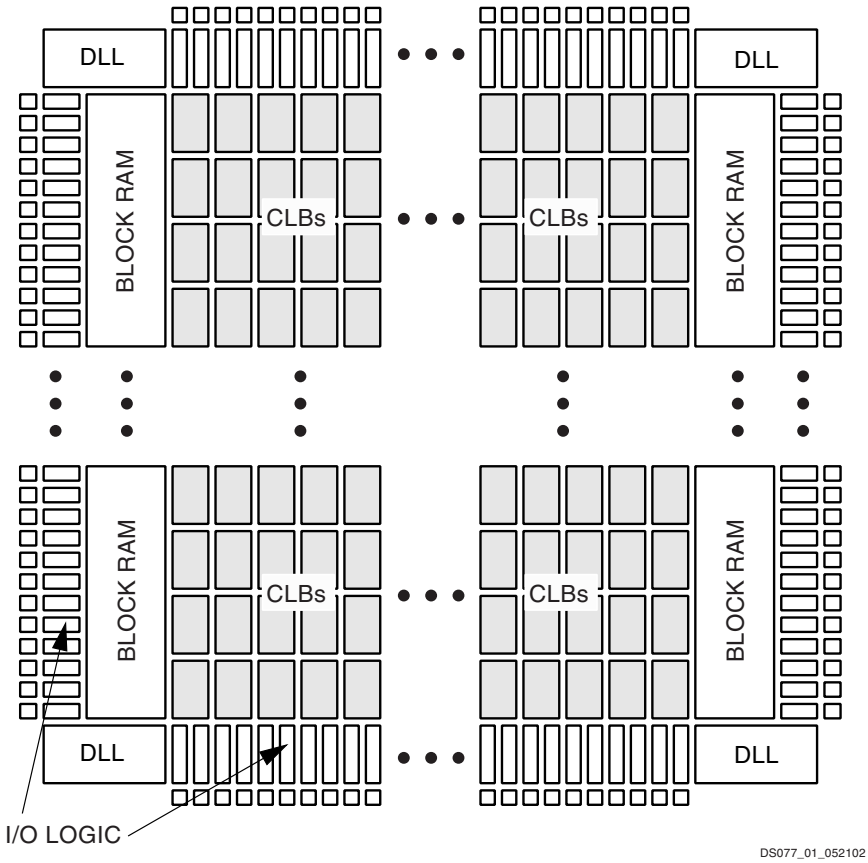


Figure 1: **Basic Spartan-IIE Family FPGA Block Diagram**

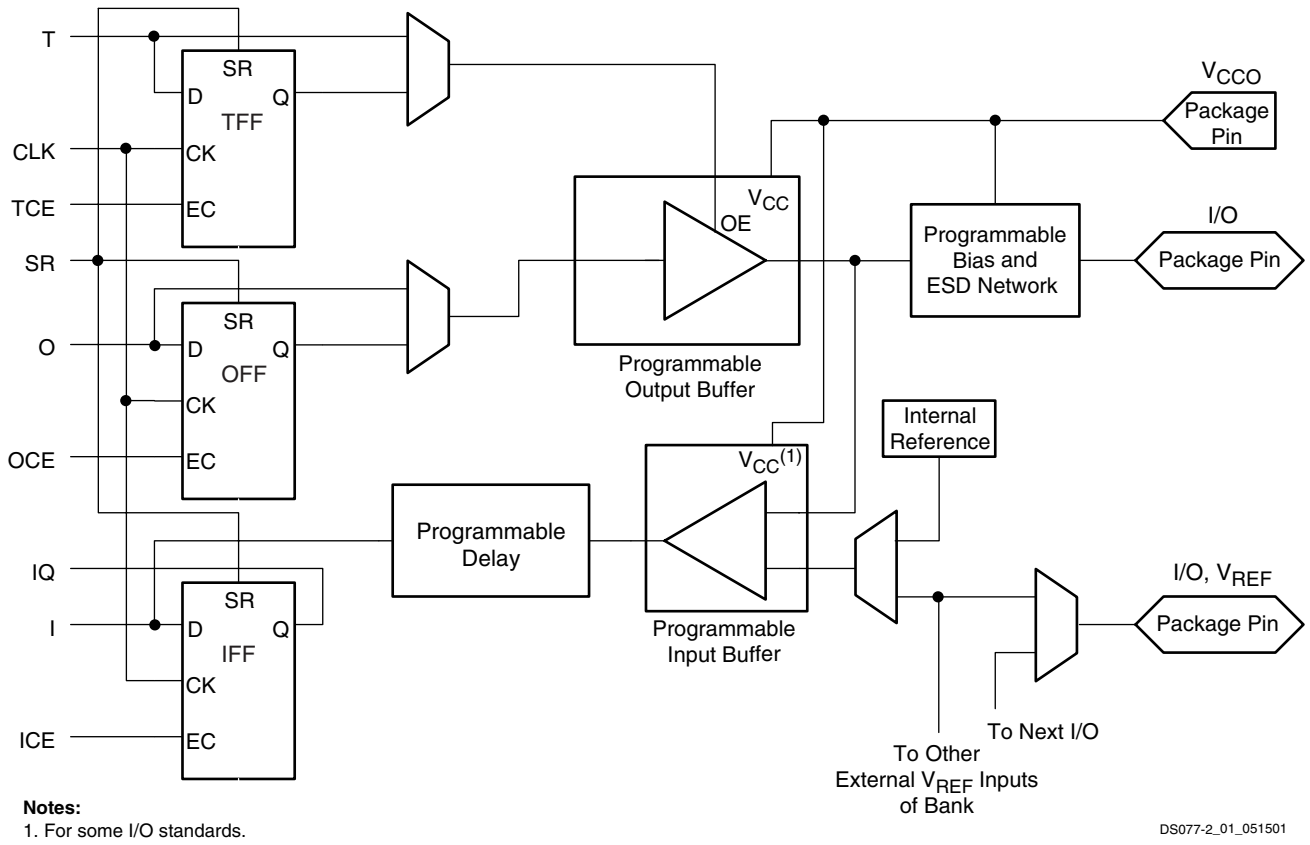


Figure 2: **Spartan-IIE Input/Output Block (IOB)**

Table 1: **Standards Supported by I/O (Typical Values)**

I/O Standard	Input Ref. Volt. (V_{REF})	Input Volt. (V_{CCO})	Output Source Volt. (V_{CCO})	Board Term. Volt. (V_{TT})
LVTTL (2-24 mA)	N/A	3.3	3.3	N/A
LVCMOS2	N/A	2.5	2.5	N/A
LVCMOS18	N/A	1.8	1.8	N/A
PCI (3V, 33 MHz/66 MHz)	N/A	3.3	3.3	N/A
GTL	0.8	N/A	N/A	1.2
GTL+	1.0	N/A	N/A	1.5
HSTL Class I	0.75	N/A	1.5	0.75
HSTL Class III	0.9	N/A	1.5	1.5
HSTL Class IV	0.9	N/A	1.5	1.5
SSTL3 Class I and II	1.5	N/A	3.3	1.5
SSTL2 Class I and II	1.25	N/A	2.5	1.25
CTT	1.5	N/A	3.3	1.5
AGP	1.32	N/A	3.3	N/A
LVDS, Bus LVDS	N/A	N/A	2.5	N/A
LVPECL	N/A	N/A	3.3	N/A

In addition to the CLK and CE control signals, the three registers share a Set/Reset (SR). For each register, this signal can be independently configured as a synchronous Set, a synchronous Reset, an asynchronous Preset, or an asynchronous Clear.

A feature not shown in the block diagram, but controlled by the software, is polarity control. The input and output buffers and all of the IOB control signals have independent polarity controls.

Optional pull-up and pull-down resistors and an optional weak-keeper circuit are attached to each user I/O pad. Prior to configuration all outputs not involved in configuration are forced into their high-impedance state. The pull-down resistors and the weak-keeper circuits are inactive, but inputs may optionally be pulled up. The activation of pull-up resistors prior to configuration is controlled on a global basis by the configuration mode pins. If the pull-up resistors are not activated, all the pins will float. Consequently, external pull-up or pull-down resistors must be provided on pins required to be at a well-defined logic level prior to configuration.

All pads are protected against damage from electrostatic discharge (ESD) and from over-voltage transients. After configuration, clamping diodes are connected to V_{CCO} for LVTTL, PCI, HSTL, SSTL, CTT, and AGP standards.

All Spartan-IIE IOBs support IEEE 1149.1-compatible boundary scan testing.

Input Path

A buffer in the Spartan-IIE IOB input path routes the input signal directly to internal logic and through an optional input flip-flop.

An optional delay element at the D-input of this flip-flop eliminates pad-to-pad hold time. The delay is matched to the internal clock-distribution delay of the FPGA, and when used, assures that the pad-to-pad hold time is zero.

Each input buffer can be configured to conform to any of the low-voltage signaling standards supported. In some of these standards the input buffer utilizes a user-supplied threshold voltage, V_{REF}. The need to supply V_{REF} imposes constraints on which standards can used in close proximity to each other. See **I/O Banking**.

There are optional pull-up and pull-down resistors at each input for use after configuration.

Output Path

The output path includes a 3-state output buffer that drives the output signal onto the pad. The output signal can be routed to the buffer directly from the internal logic or through an optional IOB output flip-flop.

The 3-state control of the output can also be routed directly from the internal logic or through a flip-flip that provides synchronous enable and disable.

Each output driver can be individually programmed for a wide range of low-voltage signaling standards. Each output buffer can source up to 24 mA and sink up to 48 mA. Drive strength and slew rate controls minimize bus transients.

In most signaling standards, the output high voltage depends on an externally supplied V_{CCO} voltage. The need to supply V_{CCO} imposes constraints on which standards can be used in close proximity to each other. See **I/O Banking**.

An optional weak-keeper circuit is connected to each output. When selected, the circuit monitors the voltage on the pad and weakly drives the pin High or Low to match the input signal. If the pin is connected to a multiple-source signal, the weak keeper holds the signal in its last state if all drivers are disabled. Maintaining a valid logic level in this way helps eliminate bus chatter.

Because the weak-keeper circuit uses the IOB input buffer to monitor the input level, an appropriate V_{REF} voltage must be provided if the signaling standard requires one. The provision of this voltage must comply with the I/O banking rules.

I/O Banking

Some of the I/O standards described above require V_{CCO} and/or V_{REF} voltages. These voltages are externally supplied and connected to device pins that serve groups of IOBs, called banks. Consequently, restrictions exist about which I/O standards can be combined within a given bank.

Eight I/O banks result from separating each edge of the FPGA into two banks (see Figure 3). The pinout tables show the bank affiliation of each I/O (see **Pinout Tables**, Module 4). Each bank has multiple V_{CCO} pins which must be connected to the same voltage. Voltage requirements are determined by the output standards in use.

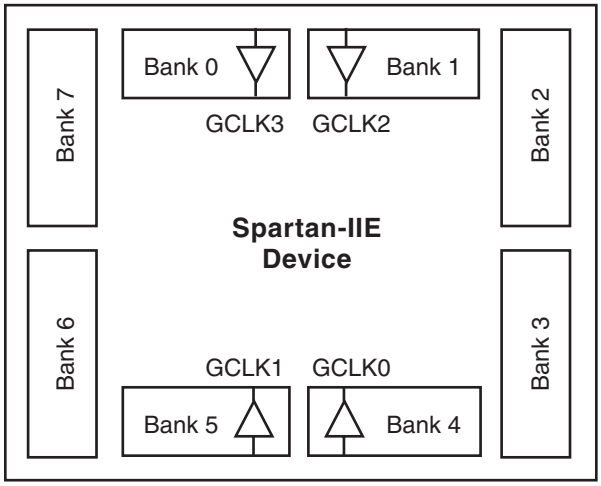


Figure 3: **Spartan-IIE I/O Banks**

In the TQ144 and PQ208 packages, the eight banks have V_{CCO} connected together. Thus, only one V_{CCO} level is allowed in these packages, although different V_{REF} values are allowed in each of the eight banks.

Within a bank, standards may be mixed only if they use the same V_{CCO}. Compatible standards are shown in Table 2. GTL and GTL+ appear under all voltages because their open-drain outputs do not depend on V_{CCO}. Note that V_{CCO} is required for most output standards and for LVTTL, LVCMOS, and PCI inputs.

Table 2: **Compatible Standards**

V_{CCO}	Compatible Standards
3.3V	PCI, LVTTL, SSTL3 I, SSTL3 II, CTT, AGP, LVPECL, GTL, GTL+
2.5V	SSTL2 I, SSTL2 II, LVCMOS2, LVDS, Bus LVDS, GTL, GTL+
1.8V	LVCMOS18, GTL, GTL+
1.5V	HSTL I, HSTL III, HSTL IV, GTL, GTL+

Some input standards require a user-supplied threshold voltage, V_{REF}. In this case, certain user-I/O pins are automatically configured as inputs for the V_{REF} voltage. About one in six of the I/O pins in the bank assume this role.

V_{REF} pins within a bank are interconnected internally and consequently only one V_{REF} voltage can be used within each bank. All V_{REF} pins in the bank, however, must be connected to the external voltage source for correct operation.

In a bank, inputs requiring V_{REF} can be mixed with those that do not but only one V_{REF} voltage may be used within a bank. The V_{CCO} and V_{REF} pins for each bank appear in the device pinout tables.

Within a given package, the number of V_{REF} and V_{CCO} pins can vary depending on the size of device. In larger devices, more I/O pins convert to V_{REF} pins. Since these are always a superset of the V_{REF} pins used for smaller devices, it is possible to design a PCB that permits migration to a larger device. All V_{REF} pins for the largest device anticipated must be connected to the V_{REF} voltage, and not used for I/O.

Table 3: **I/O Banking**

Package	TQ144, PQ208	FT256, FG456, FG676
V_{CCO} Banks	Interconnected as 1	8 independent
V_{REF} Banks	8 independent	8 independent

See Xilinx Application Note **XAPP179** for more information on I/O resources.

Hot Swap, Hot Insertion, Hot Socketing Support

The I/O pins support hot swap — also called hot insertion and hot socketing — and are considered CompactPCI Friendly according to the PCI Bus v2.2 Specification. Consequently, an unpowered Spartan-IIE FPGA can be plugged directly into a powered system or backplane without affecting or damaging the system or the FPGA. The hot swap functionality is built into every XC2S150E, XC2S400E, and XC2S600E device. All other Spartan-IIE devices built after Product Change Notice **PCN2002-05** also include hot swap functionality.

To support hot swap, Spartan-IIE devices include the following I/O features.

- Signals can be applied to Spartan-IIE I/O pins before powering the FPGA's V_{CCINT} or V_{CCO} supply inputs.
- Spartan-IIE I/O pins are high-impedance (i.e., three-stated) before and throughout the power-up and configuration processes when employing a configuration mode that does not enable the preconfiguration weak pull-up resistors (see Table 9, page 13).
- There is no current path from the I/O pin back to the V_{CCINT} or V_{CCO} voltage supplies.
- Spartan-IIE FPGAs are immune to latch-up during hot swap.

Once connected to the system, each pin adds a small amount of capacitance (C_{IN}). Likewise, each I/O consumes a small amount of DC current, equivalent to the input leakage specification (I_L). There also may be a small amount of temporary AC current (I_{HSPO}) when the pin input voltage exceeds V_{CCO} plus 0.4V, which lasts less than 10 ns.

A weak-keeper circuit within each user-I/O pin is enabled during the last frame of configuration data and has no noticeable effect on robust system signals driven by an active driver or a strong pull-up or pull-down resistor. Undriven or floating system signals may be affected. The specific effect depends on how the I/O pin is configured. User-I/O pins configured as outputs or enabled outputs have a weak pull-up resistor to V_{CCO} during the last configuration frame. User-I/O pins configured as inputs or bidirectional I/Os have weak pull-down resistors. The weak-keeper circuit turns off when the DONE pin goes High, provided that it is not used in the configured application.

Configurable Logic Block

The basic building block of the Spartan-IIE CLB is the logic cell (LC). An LC includes a 4-input function generator, carry logic, and storage element. The output from the function generator in each LC drives the CLB output or the D input of the flip-flop. Each Spartan-IIE CLB contains four LCs, organized in two similar slices; a single slice is shown in Figure 4.

In addition to the four basic LCs, the Spartan-IIE CLB contains logic that combines function generators to provide functions of five or six inputs.

Look-Up Tables

Spartan-IIE function generators are implemented as 4-input look-up tables (LUTs). In addition to operating as a function generator, each LUT can provide a 16 x 1-bit synchronous RAM. Furthermore, the two LUTs within a slice can be combined to create a 16 x 2-bit or 32 x 1-bit synchronous RAM, or a 16 x 1-bit dual-port synchronous RAM.

The Spartan-IIE LUT can also provide a 16-bit shift register that is ideal for capturing high-speed or burst-mode data. This mode can also be used to store data in applications such as Digital Signal Processing.

Storage Elements

Storage elements in the Spartan-IIE slice can be configured either as edge-triggered D-type flip-flops or as level-sensitive latches. The D inputs can be driven either by function generators within the slice or directly from slice inputs, bypassing the function generators.

In addition to Clock and Clock Enable signals, each slice has synchronous set and reset signals (SR and BY). SR forces a storage element into the initialization state specified for it in the configuration. BY forces it into the opposite state. Alternatively, these signals may be configured to operate asynchronously.

All control signals are independently invertible, and are shared by the two flip-flops within the slice.

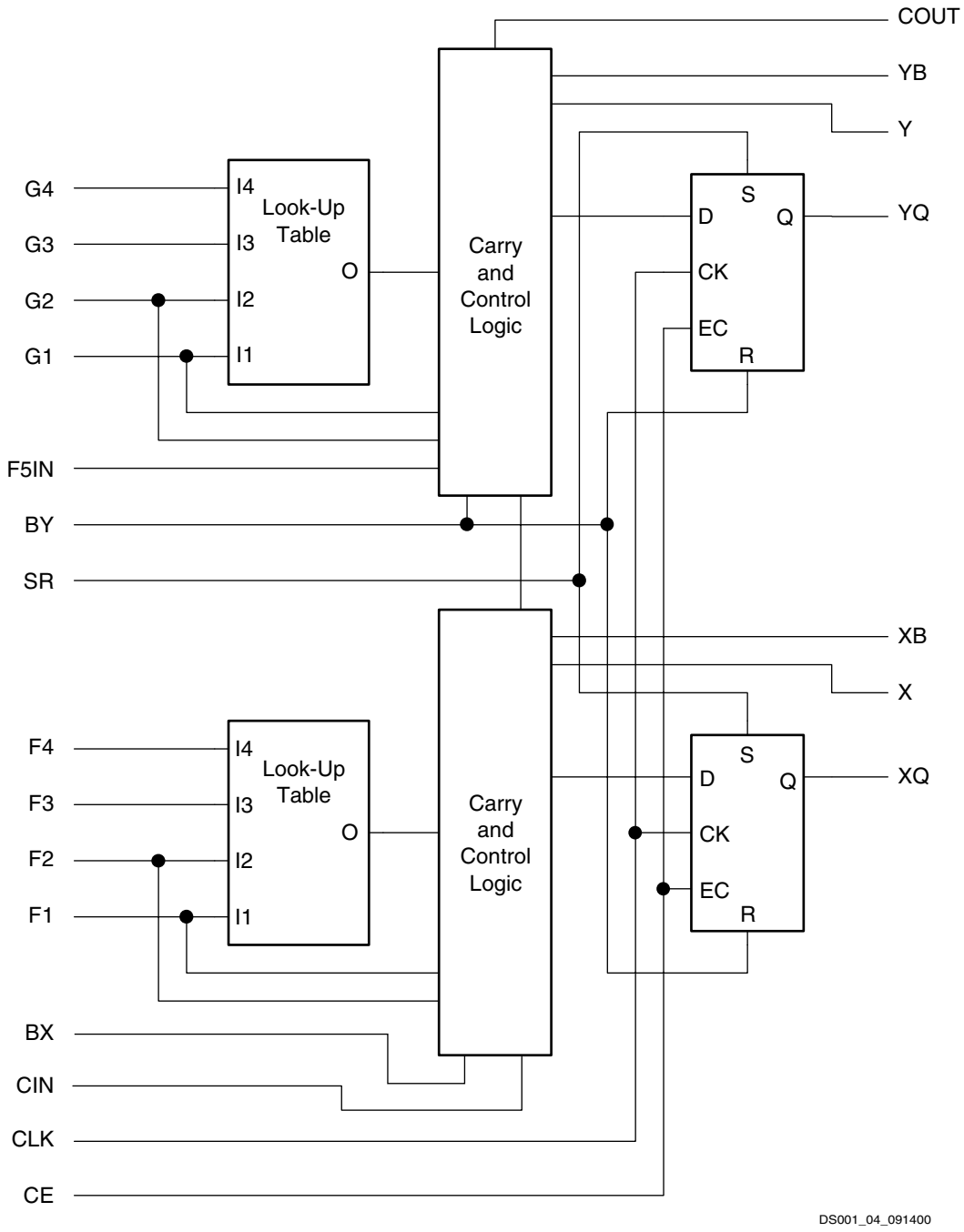


Figure 4: **Spartan-IIE CLB Slice** (two identical slices in each CLB)

Additional Logic

The F5 multiplexer in each slice combines the function generator outputs (Figure 5). This combination provides either a function generator that can implement any 5-input function, a 4:1 multiplexer, or selected functions of up to nine inputs.

Similarly, the F6 multiplexer combines the outputs of all four function generators in the CLB by selecting one of the two F5-multiplexer outputs. This permits the implementation of any 6-input function, an 8:1 multiplexer, or selected functions of up to 19 inputs.

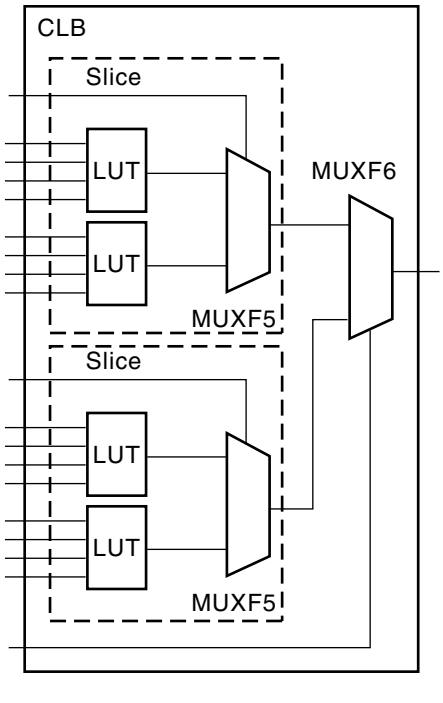


Figure 5: **F5 and F6 Multiplexers**

Each CLB has four direct feedthrough paths, one per LC. These paths provide extra data input lines or additional local routing that does not consume logic resources.

Arithmetic Logic

Dedicated carry logic provides fast arithmetic carry capability for high-speed arithmetic functions. The Spartan-IIE CLB supports two separate carry chains, one per slice. The height of the carry chains is two bits per CLB.

The arithmetic logic includes an XOR gate that allows a 1-bit full adder to be implemented within an LC. In addition, a dedicated AND gate improves the efficiency of multiplier implementations.

The dedicated carry path can also be used to cascade function generators for implementing wide logic functions.

BUFTs

Each Spartan-IIE CLB contains two 3-state drivers (BUFTs) that can drive on-chip busses. The IOBs on the left and right sides can also drive the on-chip busses. See **Dedicated Routing**, page 8. Each Spartan-IIE BUFT has an independent 3-state control pin and an independent input pin. The 3-state control pin is an active-Low enable (T). When all BUFTs on a net are disabled, the net is High. There is no need to instantiate a pull-up unless desired for simulation purposes. Simultaneously driving BUFTs onto the same net will not cause contention. If driven both High and Low, the net will be Low.

Block RAM

Spartan-IIE FPGAs incorporate several large block RAM memories. These complement the distributed RAM Look-Up Tables (LUTs) that provide shallow memory structures implemented in CLBs.

Block RAM memory blocks are organized in columns. Most Spartan-IIE devices contain two such columns, one along each vertical edge. The XC2S400E has four block RAM columns and the XC2S600E has six block RAM columns. These columns extend the full height of the chip. Each memory block is four CLBs high, and consequently, a Spartan-IIE device 16 CLBs high will contain four memory blocks per column, and a total of eight blocks.

Table 4: **Spartan-IIE Block RAM Amounts**

Spartan-IIE Device	# of Blocks	Total Block RAM Bits
XC2S50E	8	32K
XC2S100E	10	40K
XC2S150E	12	48K
XC2S200E	14	56K
XC2S300E	16	64K
XC2S400E	40	160K
XC2S600E	72	288K

Each block RAM cell, as illustrated in Figure 6, is a fully synchronous dual-ported 4096-bit RAM with independent control signals for each port. The data widths of the two ports can be configured independently, providing built-in bus-width conversion.

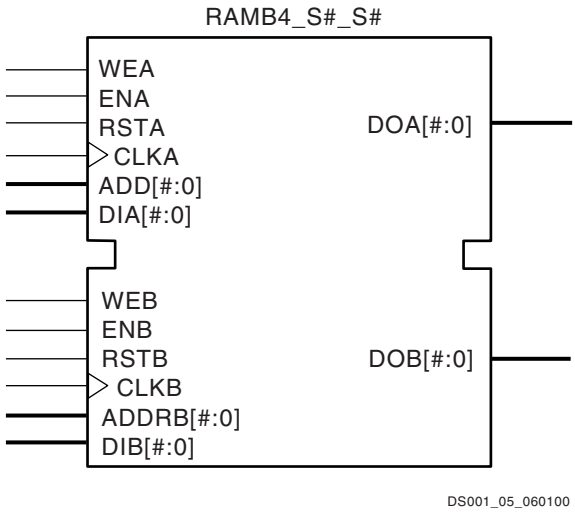


Figure 6: **Dual-Port Block RAM**

Table 5 shows the depth and width aspect ratios for the block RAM.

Table 5: **Block RAM Port Aspect Ratios**

Width	Depth	ADDR Bus	Data Bus
1	4096	ADDR<11:0>	DATA<0>
2	2048	ADDR<10:0>	DATA<1:0>
4	1024	ADDR<9:0>	DATA<3:0>
8	512	ADDR<8:0>	DATA<7:0>
16	256	ADDR<7:0>	DATA<15:0>

The Spartan-IIE block RAM also includes dedicated routing to provide an efficient interface with both CLBs and other block RAMs. See Xilinx Application Note **XAPP173** for more information on block RAM.

Programmable Routing

It is the longest delay path that limits the speed of any design. Consequently, the Spartan-IIE routing architecture and its place-and-route software were defined jointly to minimize long-path delays and yield the best system performance.

The joint optimization also reduces design compilation times because the architecture is software-friendly. Design cycles are correspondingly reduced due to shorter design iteration times.

The software automatically uses the best available routing based on user timing requirements. The details are provided here for reference.

Local Routing

The local routing resources, as shown in Figure 7, provide the following three types of connections:

- Interconnections among the LUTs, flip-flops, and General Routing Matrix (GRM), described below.
- Internal CLB feedback paths that provide high-speed connections to LUTs within the same CLB, chaining them together with minimal routing delay
- Direct paths that provide high-speed connections between horizontally adjacent CLBs, eliminating the delay of the GRM

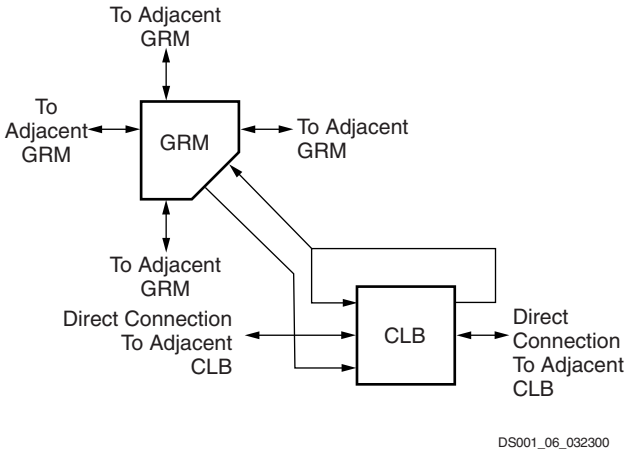


Figure 7: **Spartan-IIE Local Routing**

General Purpose Routing

Most Spartan-IIE signals are routed on the general purpose routing, and consequently, the majority of interconnect resources are associated with this level of the routing hierarchy. The general routing resources are located in horizontal and vertical routing channels associated with the rows and columns of CLBs. The general-purpose routing resources are listed below.

- Adjacent to each CLB is a General Routing Matrix (GRM). The GRM is the switch matrix through which horizontal and vertical routing resources connect, and is also the means by which the CLB gains access to the general purpose routing.
- 24 single-length lines route GRM signals to adjacent GRMs in each of the four directions.
- 96 buffered Hex lines route GRM signals to other GRMs six blocks away in each one of the four directions. Organized in a staggered pattern, Hex lines may be driven only at their endpoints. Hex-line signals can be accessed either at the endpoints or at the midpoint (three blocks from the source). One third of the Hex lines are bidirectional, while the remaining ones are unidirectional.
- 12 Longlines are buffered, bidirectional wires that distribute signals across the device quickly and efficiently. Vertical Longlines span the full height of the device, and horizontal ones span the full width of the device.

I/O Routing

Spartan-IIE devices have additional routing resources around their periphery that form an interface between the CLB array and the IOBs. This additional routing, called the VersaRing™ routing, facilitates pin-swapping and pin-locking, such that logic redesigns can adapt to existing PCB layouts. Time-to-market is reduced, since PCBs and other system components can be manufactured while the logic design is still in progress.

Dedicated Routing

Some classes of signal require dedicated routing resources to maximize performance. In the Spartan-IIE architecture, dedicated routing resources are provided for two classes of signal.

- Horizontal routing resources are provided for on-chip 3-state busses. Four partitionable bus lines are provided per CLB row, permitting multiple busses within a row, as shown in Figure 8.
- Two dedicated nets per CLB propagate carry signals vertically to the adjacent CLB.

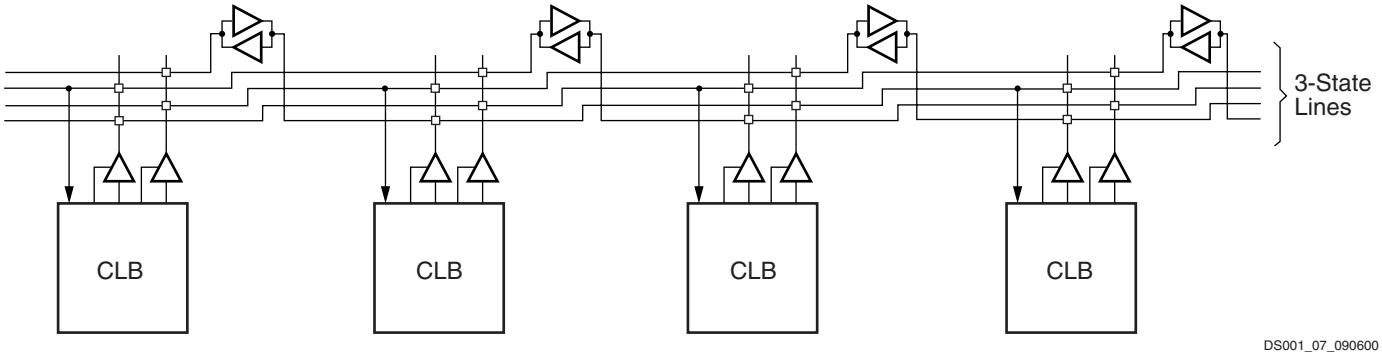


Figure 8: **BUFT Connections to Dedicated Horizontal Bus Lines**

Global Routing

Global Routing resources distribute clocks and other signals with very high fanout throughout the device. Spartan-IIE devices include two tiers of global routing resources referred to as primary and secondary global routing resources.

- The primary global routing resources are four dedicated global nets with dedicated input pins that are designed to distribute high-fanout clock signals with minimal skew. Each global clock net can drive all CLB, IOB, and block RAM clock pins. The primary global nets may only be driven by global buffers. There are four global buffers, one for each global net.
- The secondary global routing resources consist of 24 backbone lines, 12 across the top of the chip and 12 across the bottom. From these lines, up to 12 unique signals per column can be distributed via the 12 longlines in the column. These secondary resources are more flexible than the primary resources since they are not restricted to routing only to clock pins.

Clock Distribution

The Spartan-IIE family provides high-speed, low-skew clock distribution through the primary global routing resources described above. A typical clock distribution net is shown in Figure 9.

Four global buffers are provided, two at the top center of the device and two at the bottom center. These drive the four primary global nets that in turn drive any clock pin.

Four dedicated clock pads are provided, one adjacent to each of the global buffers. The input to the global buffer is selected either from these pads or from signals in the general purpose routing.

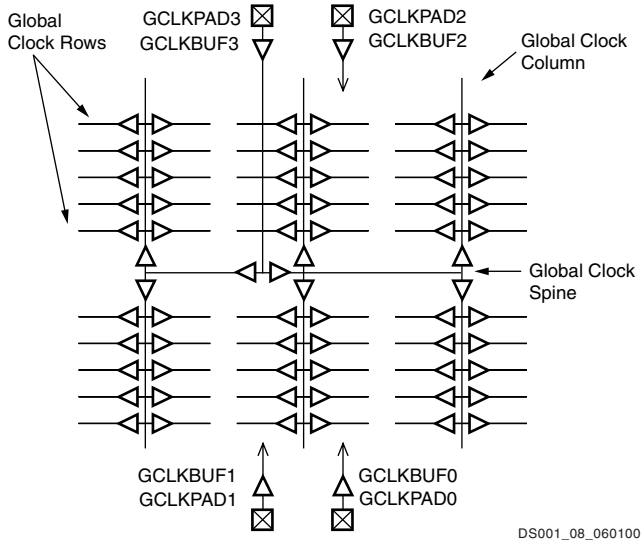


Figure 9: **Global Clock Distribution Network**

Delay-Locked Loop (DLL)

Associated with each global clock input buffer is a fully digital Delay-Locked Loop (DLL) that can eliminate skew between the clock input pad and internal clock-input pins throughout the device. Each DLL can drive two global clock networks. The DLL monitors the input clock and the distributed clock, and automatically adjusts a clock delay element (Figure 10). Additional delay is introduced such that clock edges reach internal flip-flops exactly one clock period after they arrive at the input. This closed-loop system effectively eliminates clock-distribution delay by ensuring that clock

edges arrive at internal flip-flops in synchronism with clock edges arriving at the input.

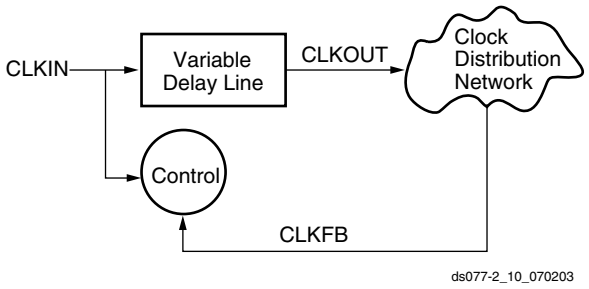


Figure 10: **Delay-Locked Loop Block Diagram**

In addition to eliminating clock-distribution delay, the DLL provides advanced control of multiple clock domains. The DLL provides four quadrature phases of the source clock, can double the clock, or divide the clock by 1.5, 2, 2.5, 3, 4, 5, 8, or 16. The phase-shifted output have optional duty-cycle correction (Figure 11).

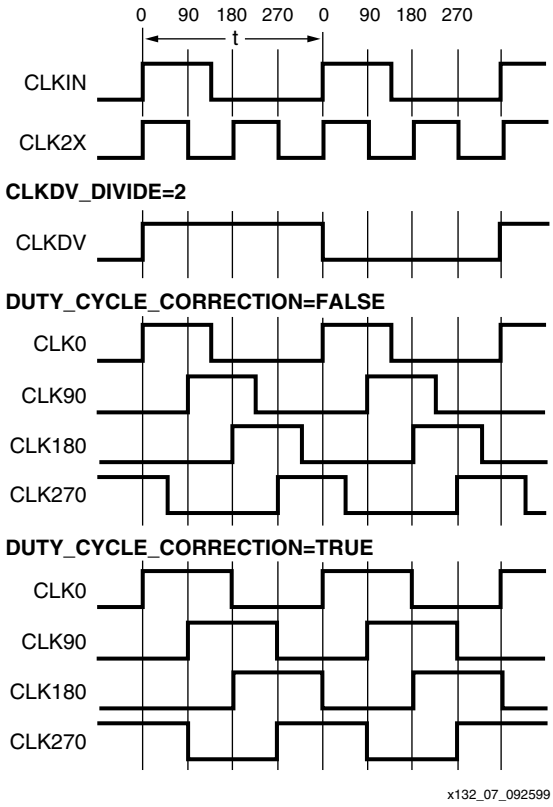


Figure 11: **DLL Output Characteristics**

The DLL also operates as a clock mirror. By driving the output from a DLL off-chip and then back on again, the DLL can be used to deskew a board level clock among multiple Spartan-IIE devices.

In order to guarantee that the system clock is operating correctly prior to the FPGA starting up after configuration, the DLL can delay the completion of the configuration process until after it has achieved lock. If the DLL uses external feedback, apply a reset after startup to ensure consistent locking to the external signal. See Xilinx Application Note **XAPP174** for more information on DLLs.

Boundary Scan

Spartan-IIE devices support all the mandatory boundary-scan instructions specified in the IEEE standard 1149.1. A Test Access Port (TAP) and registers are provided that implement the EXTEST, INTEST, SAMPLE/PRELOAD, BYPASS, IDCODE, and HIGHZ instructions. The TAP also supports two USERCODE instructions, internal scan chains, and configuration/readback of the device.

The TAP uses dedicated package pins that always operate using LVTTL. For TDO to operate using LVTTL, the V_{CCO} for Bank 2 must be 3.3V. Otherwise, TDO switches rail-to-rail between ground and V_{CCO}. The boundary-scan input pins (TDI, TMS, TCK) do not have a V_{CCO} requirement and operate with either 2.5V or 3.3V input signalling levels.

Boundary-scan operation is independent of individual IOB configurations, and unaffected by package type. All IOBs, including unbonded ones, are treated as independent 3-state bidirectional pins in a single scan chain. Retention of the bidirectional test capability after configuration facilitates the testing of external interconnections.

Table 6 lists the boundary-scan instructions supported in Spartan-IIE FPGAs. Internal signals can be captured during EXTEST by connecting them to unbonded or unused IOBs. They may also be connected to the unused outputs of IOBs defined as unidirectional input pins.

Table 6: **Boundary-Scan Instructions**

Boundary-Scan Command	Binary Code[4:0]	Description
EXTEST	00000	Enables boundary-scan EXTEST operation
SAMPLE/ PRELOAD	00001	Enables boundary-scan SAMPLE/PRELOAD operation
USER1	00010	Access user-defined register 1
USER2	00011	Access user-defined register 2
CFG_OUT	00100	Access the configuration bus for Readback
CFG_IN	00101	Access the configuration bus for Configuration
INTEST	00111	Enables boundary-scan INTEST operation

Table 6: **Boundary-Scan Instructions *(Continued)***

Boundary-Scan Command	Binary Code[4:0]	Description
USERCODE	01000	Enables shifting out USER code
IDCODE	01001	Enables shifting out of ID Code
HIGHZ	01010	Disables output pins while enabling the Bypass Register
JSTART	01100	Clock the start-up sequence when StartupClk is TCK
BYPASS	11111	Enables BYPASS
RESERVED	All other codes	Xilinx reserved instructions

The public boundary-scan instructions are available prior to configuration, except for USER1 and USER2. After configuration, the public instructions remain available together with any USERCODE instructions installed during the configuration. While the SAMPLE/PRELOAD and BYPASS instructions are available during configuration, it is recommended that boundary-scan operations not be performed during this transitional period.

In addition to the test instructions outlined above, the boundary-scan circuitry can be used to configure the FPGA, and also to read back the configuration data.

To facilitate internal scan chains, the User Register provides three outputs (Reset, Update, and Shift) that represent the corresponding states in the boundary-scan internal state machine.

Figure 12 is a diagram of the Spartan-IIE family boundary scan logic. It includes three bits of Data Register per IOB, the IEEE 1149.1 Test Access Port controller, and the Instruction Register with decodes.

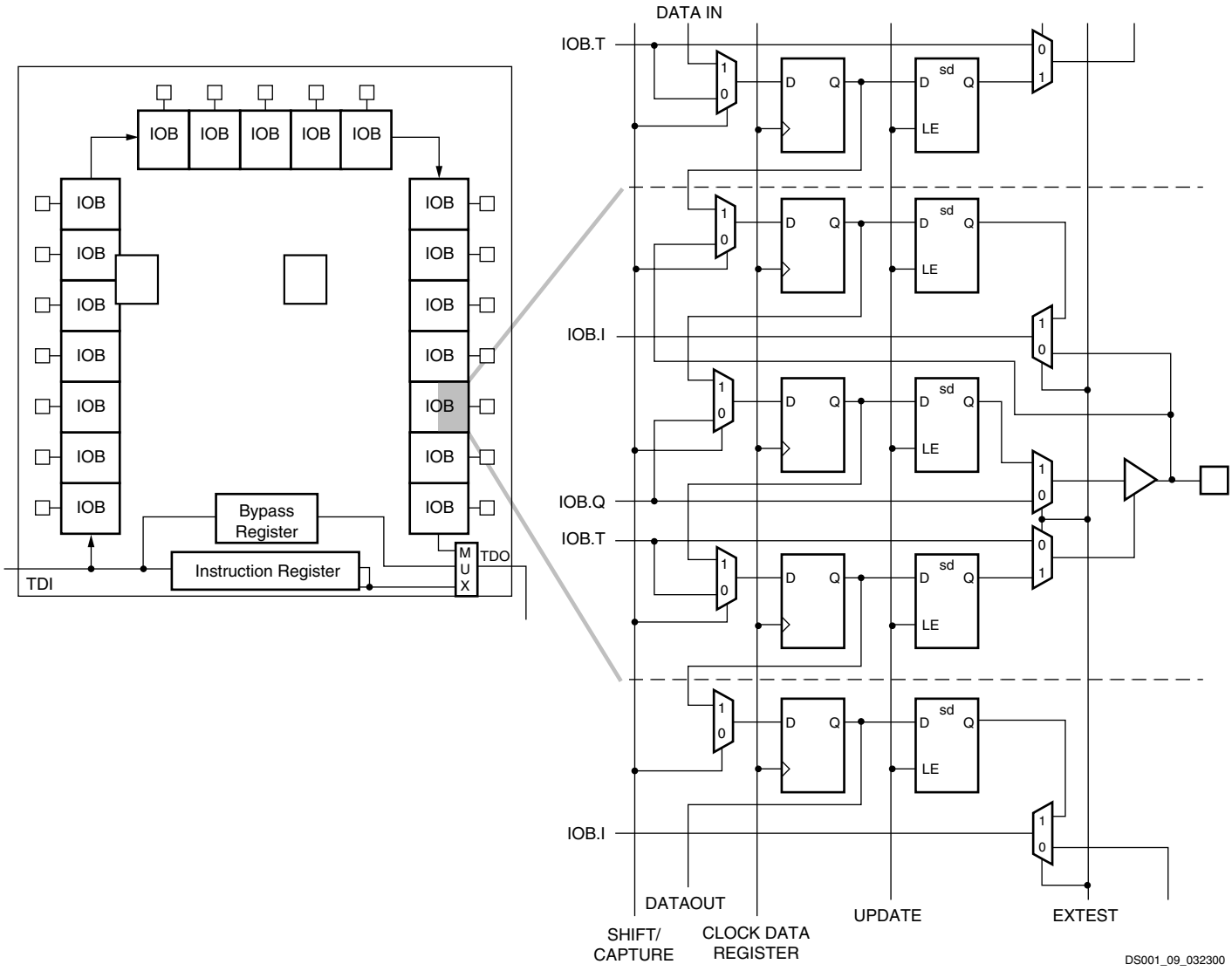


Figure 12: **Spartan-IIE Family Boundary Scan Logic**

Bit Sequence

The bit sequence within each IOB is: In, Out, 3-State. The input-only pins contribute only the In bit to the boundary scan I/O data register, while the output-only pins contributes all three bits.

From a cavity-up view of the chip (as shown in the FPGA Editor), starting in the upper right chip corner, the boundary scan data-register bits are ordered as shown in Figure 13.

BSDL (Boundary Scan Description Language) files for Spartan-IIE family devices are available on the Xilinx web site at **http://www.xilinx.com/support/sw_bsdl.htm**.

Spartan-IIE boundary scan IDCODE values are shown in Table 7.

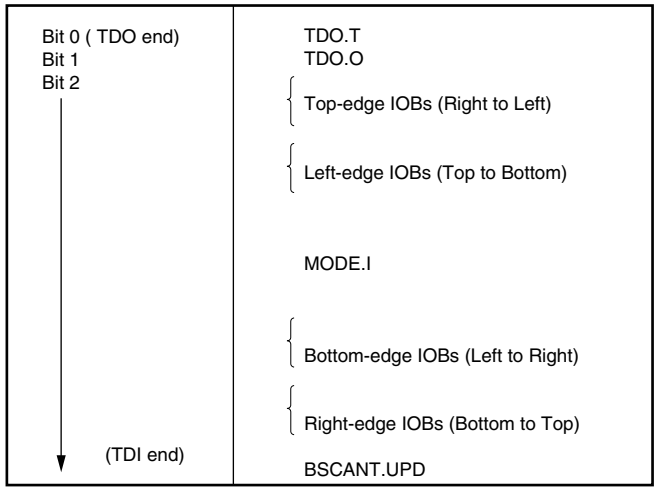


Figure 13: **Boundary Scan Bit Sequence**

Table 7: **Spartan-IIE IDCODE Values**

Device	IDCODE				
	Version	Family	Array Size	Manufacturer	Required
XC2S50E	XXXX	0000 101	0 0001 0000	0000 1001 001	1
XC2S100E	XXXX	0000 101	0 0001 0100	0000 1001 001	1
XC2S150E	XXXX	0000 101	0 0001 1000	0000 1001 001	1
XC2S200E	XXXX	0000 101	0 0001 1100	0000 1001 001	1
XC2S300E	XXXX	0000 101	0 0010 0000	0000 1001 001	1
XC2S400E	XXXX	0000 101	0 0010 1000	0000 1001 001	1
XC2S600E	XXXX	0000 101	0 0011 0000	0000 1001 001	1

Development System

Spartan-IIE FPGAs are supported by the Xilinx ISE Foundation and Alliance CAE tools. The basic methodology for Spartan-IIE design consists of three interrelated steps: design entry, implementation, and verification. Industry-standard tools are used for design entry and simulation, while Xilinx provides proprietary architecture-specific tools for implementation.

The Xilinx development system is integrated under the Xilinx Project Navigator software, providing designers with a common user interface regardless of their choice of entry and verification tools. The software simplifies the selection of implementation options with pull-down menus and on-line help.

Application programs ranging from schematic capture to placement and routing can be accessed through the software. The program command sequence is generated prior to execution, and stored for documentation.

Several advanced software features facilitate Spartan-IIE design. CORE Generator™ functions, for example, include macros with relative location constraints to guide their placement. They help ensure optimal implementation of common functions.

For HDL design entry, the Xilinx FPGA development system provides interfaces to several synthesis design environments.

A standard interface-file specification, Electronic Design Interchange Format (EDIF), simplifies file transfers into and out of the development system.

Spartan-IIE FPGAs are supported by a unified library of standard functions. This library contains over 400 primitives and macros, ranging from 2-input AND gates to 16-bit accumulators, and includes arithmetic functions, comparators, counters, data registers, decoders, encoders, I/O functions, latches, Boolean functions, multiplexers, shift registers, and barrel shifters.

The design environment supports hierarchical design entry, with high-level designs that comprise major functional blocks, while lower-level designs define the logic in these blocks. These hierarchical design elements are automatically combined by the implementation tools. Different design entry tools can be combined within a hierarchical design, thus allowing the most convenient entry method to be used for each portion of the design.

Design Implementation

The place-and-route tools automatically provide the implementation flow described in this section. The partitioner takes the EDIF netlist for the design and maps the logic into the architectural resources of the FPGA (CLBs and IOBs, for example). The placer then determines the best locations for these blocks based on their interconnections and the desired performance. Finally, the router interconnects the blocks.

The algorithms support fully automatic implementation of most designs. For demanding applications, however, the user can exercise various degrees of control over the process. User partitioning, placement, and routing information is optionally specified during the design-entry process. The implementation of highly structured designs can benefit greatly from basic floorplanning.

The implementation software incorporates timing-driven placement and routing. Designers specify timing requirements along entire paths during design entry. The timing path analysis routines then recognize these user-specified requirements and accommodate them.

Timing requirements are entered in a form directly relating to the system requirements, such as the targeted clock frequency, or the maximum allowable delay between two registers. In this way, the overall performance of the system along entire signal paths is automatically tailored to user-generated specifications. Specific timing information for individual nets is unnecessary.

Design Verification

In addition to conventional software simulation, FPGA users can use in-circuit debugging techniques. Because Xilinx devices are infinitely reprogrammable, designs can be verified in real time without the need for extensive sets of software simulation vectors.

The development system supports both software simulation and in-circuit debugging techniques. For simulation, the system extracts the post-layout timing information from the design database, and back-annotates this information into the netlist for use by the simulator. Alternatively, the user can verify timing-critical portions of the design using the static timing analyzer.

For in-circuit debugging, Xilinx offers a download and readback cable, which connects the FPGA in the target system to a PC or workstation. After downloading the design into the FPGA, the designer can single-step the logic, readback the contents of the flip-flops, and so observe the internal logic state. Simple modifications can be downloaded into the system in a matter of minutes.

Configuration

Configuration is the process by which the bitstream of a design, as generated by the Xilinx development software, is loaded into the internal configuration memory of the FPGA. Spartan-IIE devices support both serial configuration, using the master/slave serial and JTAG modes, as well as byte-wide configuration employing the Slave Parallel mode.

Configuration File

Spartan-IIE devices are configured by sequentially loading frames of data that have been concatenated into a configuration file. Table 8 shows how much nonvolatile storage space is needed for Spartan-IIE devices.

It is important to note that, while a PROM is commonly used to store configuration data before loading them into the FPGA, it is by no means required. Any of a number of different kinds of under populated nonvolatile storage already available either on or off the board (for example, hard drives, FLASH cards, and so on) can be used.

Table 8: **Spartan-IIE Configuration File Size**

Device	Configuration File Size (Bits)
XC2S50E	630,048
XC2S100E	863,840
XC2S150E	1,134,496
XC2S200E	1,442,016
XC2S300E	1,875,648
XC2S400E	2,693,440
XC2S600E	3,961,632

Modes

Spartan-IIE devices support the following four configuration modes:

- Slave Serial mode
- Master Serial mode
- Slave Parallel mode
- Boundary-scan mode

The Configuration mode pins (M2, M1, M0) select among these configuration modes with the option in each case of having the IOB pins either pulled up or left floating prior to configuration. The selection codes are listed in Table 9.

Configuration through the boundary-scan port is always available, independent of the mode selection. Selecting the boundary-scan mode simply turns off the other modes. The three mode pins have internal pull-up resistors, and default to a logic High if left unconnected.

Table 9: **Configuration Modes**

Configuration Mode	Preconfiguration Pull-ups	M0	M1	M2	CCLK Direction	Data Width	Serial D_{OUT}
Master Serial mode	No	0	0	0	Out	1	Yes
	Yes	0	0	1			
Slave Parallel mode (SelectMAP)	Yes	0	1	0	In	8	No
	No	0	1	1			
Boundary-Scan mode	Yes	1	0	0	N/A	1	No
	No	1	0	1			
Slave Serial mode	Yes	1	1	0	In	1	Yes
	No	1	1	1			

Signals

There are two kinds of pins that are used to configure Spartan-IIE devices: Dedicated pins perform only specific configuration-related functions; the other pins can serve as general purpose I/Os once user operation has begun.

The dedicated pins comprise the mode pins (M2, M1, M0), the configuration clock pin (CCLK), the $\overline{\text{PROGRAM}}$ pin, the DONE pin and the boundary-scan pins (TDI, TDO, TMS, TCK). Depending on the selected configuration mode, CCLK may be an output generated by the FPGA, or may be generated externally, and provided to the FPGA as an input.

Note that some configuration pins can act as outputs. For correct operation, these pins require a V_{CCO} of 3.3V to drive an LVTTL signal or 2.5V to drive an LVCMOS signal. All the relevant pins fall in banks 2 or 3. The $\overline{\text{CS}}$ and $\overline{\text{WRITE}}$ pins for Slave Parallel mode are located in bank 1.

For a more detailed description than that given below, see ***Spartan-IIE 1.8V FPGA Family: Pinout Tables*** and **XAPP176**, *Spartan-II FPGA Series Configuration and Readback*.

The Process

The sequence of steps necessary to configure Spartan-IIE devices are shown in Figure 14. The overall flow can be divided into three different phases.

- Initiating configuration
- Configuration memory clear
- Loading data frames
- Start-up

The memory clearing and start-up phases are the same for all configuration modes; however, the steps for the loading of data frames are different. Thus, the details for data frame loading are described separately in the sections devoted to each mode.

Initiating Configuration

There are two different ways to initiate the configuration process: applying power to the device or asserting the $\overline{\text{PROGRAM}}$ input.

Configuration on power-up occurs automatically unless it is delayed by the user, as described in a separate section below. The waveform for configuration on power-up is shown in ***Spartan-IIE 1.8V FPGA Family: DC and Switching Characteristics***. Before configuration can begin, V_{CCO} Bank 2 must be greater than 1.0V. Furthermore, all V_{CCINT} power pins must be connected to a 1.8V supply. For more information on delaying configuration, see **Clearing Configuration Memory**, page 14.

Once in user operation, the device can be re-configured simply by pulling the $\overline{\text{PROGRAM}}$ pin Low. The device acknowledges the beginning of the configuration process by driving DONE Low, then enters the memory-clearing phase.

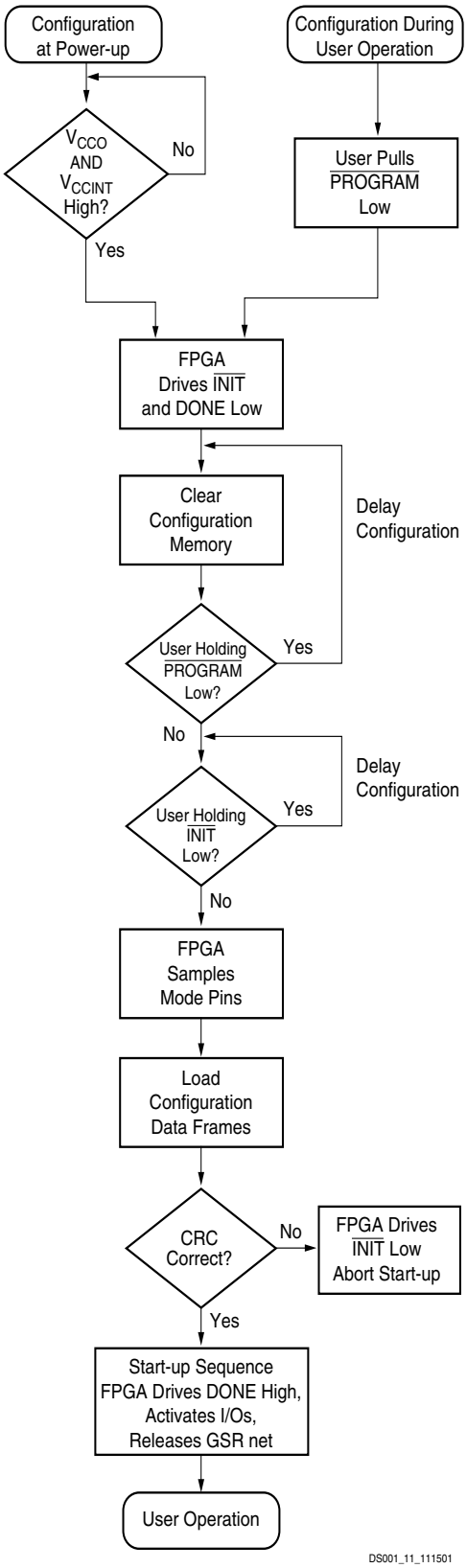


Figure 14: **Configuration Flow Diagram**

Clearing Configuration Memory

The device indicates that clearing the configuration memory is in progress by driving $\overline{\text{INIT}}$ Low.

Delaying Configuration

At this time, the user can delay configuration by holding either $\overline{\text{PROGRAM}}$ or $\overline{\text{INIT}}$ Low, which causes the device to remain in the memory clearing phase. Note that the bidirectional $\overline{\text{INIT}}$ line is driving a Low logic level during memory clearing. Thus, to avoid contention, use an open-drain driver to keep $\overline{\text{INIT}}$ Low.

With no delay in force, the device indicates that the memory is completely clear by driving $\overline{\text{INIT}}$ High. The FPGA samples its mode pins on this Low-to-High transition.

Loading Configuration Data

Once $\overline{\text{INIT}}$ is High, the user can begin loading configuration data frames into the device. The details of loading the configuration data are discussed in the sections treating the configuration modes individually. The sequence of operations necessary to load configuration data using the serial modes is shown in Figure 16. Loading data using the Slave Parallel mode is shown in Figure 19, page 19.

CRC Error Checking

After the loading of configuration data, a CRC value embedded in the configuration file is checked against a CRC value calculated within the FPGA. If the CRC values do not match, the FPGA drives $\overline{\text{INIT}}$ Low to indicate that an error has occurred and configuration is aborted. Note that attempting to load an incorrect bitstream causes configuration to fail and can damage the device.

To reconfigure the device, the $\overline{\text{PROGRAM}}$ pin should be asserted to reset the configuration logic. Recycling power also resets the FPGA for configuration. See **Clearing Configuration Memory**.

Start-up

The start-up sequence oversees the transition of the FPGA from the configuration state to full user operation. A match of CRC values, indicating a successful loading of the configuration data, initiates the sequence.

During start-up, the device performs four operations:

1. The assertion of DONE. The failure of DONE to go High may indicate the unsuccessful loading of configuration data.
2. The release of the Global Three State (GTS). This activates all the I/Os.
3. The release of the Global Set Reset (GSR). This allows all flip-flops to change state.
4. The assertion of Global Write Enable (GWE). This allows all RAMs and flip-flops to change state.

By default, these operations are synchronized to CCLK. The entire start-up sequence lasts eight cycles, called C0-C7, after which the loaded design is fully functional. The four operations can be selected to switch on any CCLK cycle C1-C6 through settings in the Xilinx Development Software. The default timing for start-up is shown in the top half of Figure 15; heavy lines show default settings.

The default Start-up sequence is that one CCLK cycle after DONE goes High, the global 3-state signal (GTS) is released. This permits device outputs to turn on as necessary.

One CCLK cycle later, the Global Set/Reset (GSR) and Global Write Enable (GWE) signals are released. This permits the internal storage elements to begin changing state in response to the logic and the user clock.

The bottom half of Figure 15 shows another commonly used version of the start-up timing known as Sync-to-DONE. This version makes the GTS, GSR, and GWE events conditional upon the DONE pin going High. This timing is important for a daisy chain of multiple FPGAs in serial mode, since it ensures that all FPGAs go through start-up together, after all their DONE pins have gone High.

Sync-to-DONE timing is selected by setting the GTS, GSR, and GWE cycles to a value of DONE in the configuration options. This causes these signals to transition one clock cycle after DONE externally transitions High.

The sequence can also be paused at any stage until lock has been achieved on any or all DLLs.

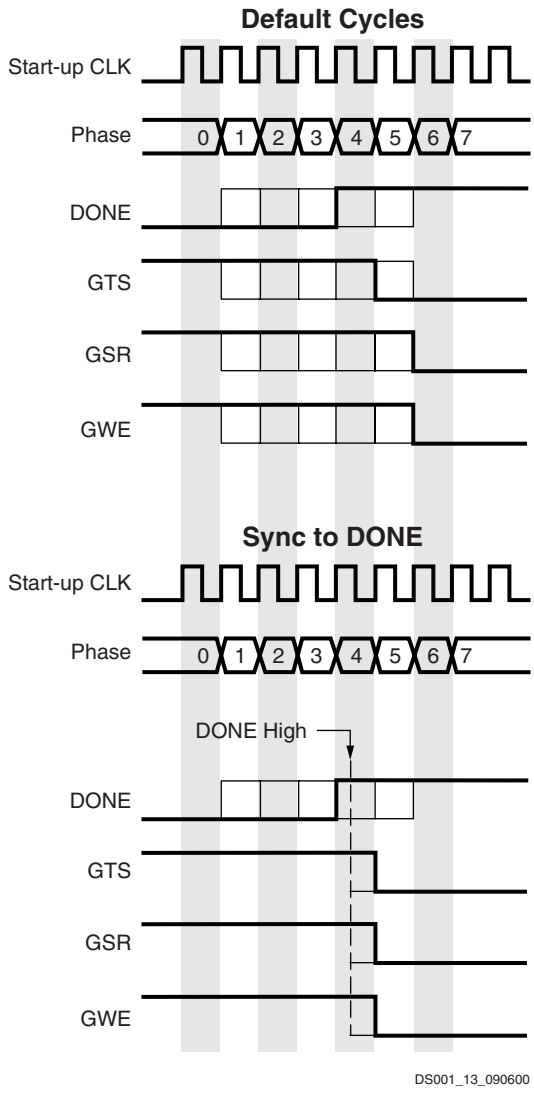


Figure 15: **Start-Up Waveforms**

Serial Modes

There are two serial configuration modes. In Master Serial mode, the FPGA controls the configuration process by driving CCLK as an output. In Slave Serial mode, the FPGA passively receives CCLK as an input from an external agent (e.g., a microprocessor, CPLD, or second FPGA in master mode) that is controlling the configuration process. In both modes, the FPGA is configured by loading one bit per CCLK cycle. The MSB of each configuration data byte is always written to the DIN pin first.

See Figure 16 for the sequence for loading data into the Spartan-IIE FPGA serially. This is an expansion of the "Load Configuration Data Frames" block in Figure 14, page 14.

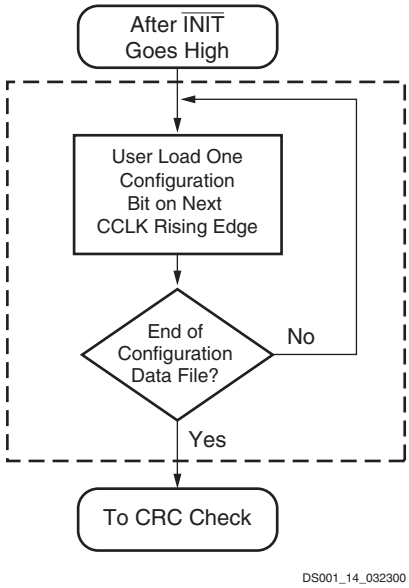


Figure 16: **Loading Serial Mode Configuration Data**

Slave Serial Mode

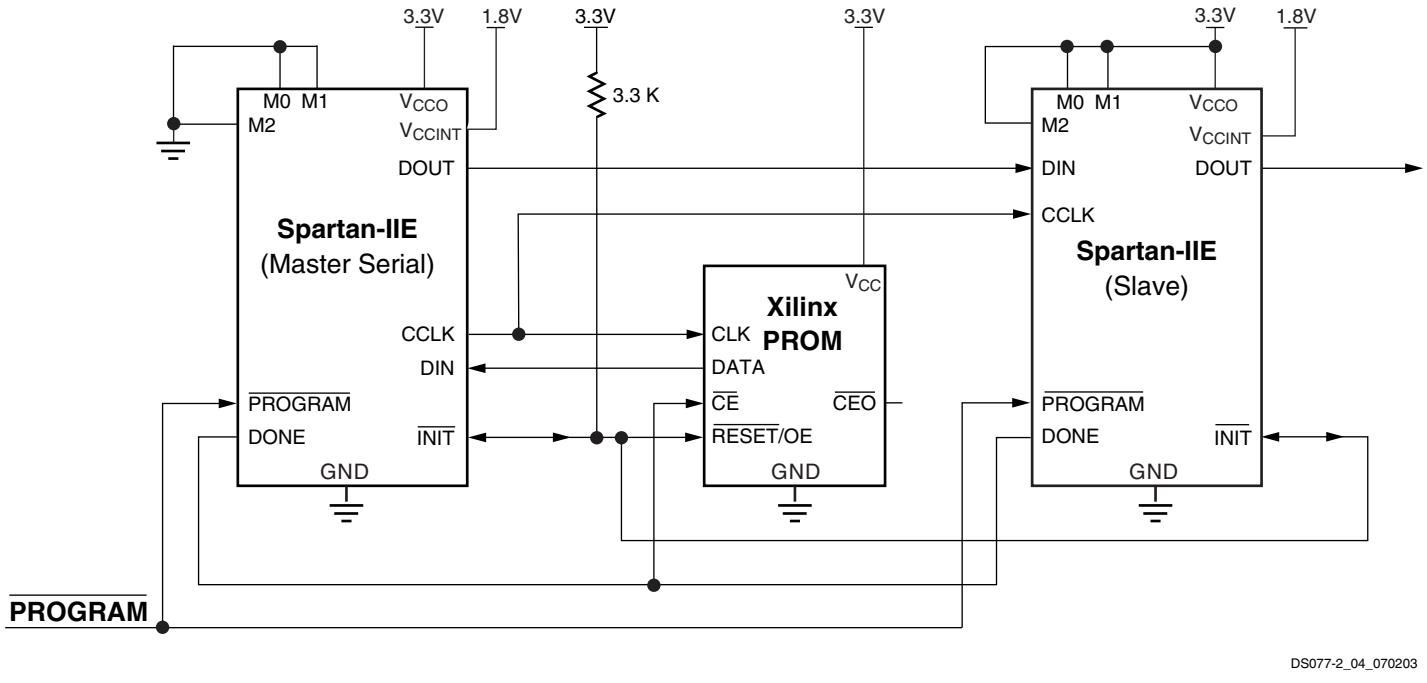
In Slave Serial mode, the FPGA's CCLK pin is driven by an external source, allowing the FPGA to be configured from other logic devices such as microprocessors or in a daisy-chain configuration. Figure 17 shows connections for a Master Serial FPGA configuring a Slave Serial FPGA from a PROM. A Spartan-IIE device in slave serial mode should be connected as shown for the third device from the left. Slave Serial mode is selected by a <11x> on the mode pins (M0, M1, M2). The weak pull-ups on the mode pins make slave serial the default mode if the pins are left unconnected.

The serial bitstream must be setup at the DIN input pin a short time before each rising edge of an externally generated CCLK.

Timing for Slave Serial mode is shown in ***Spartan-IIE 1.8V FPGA Family: DC and Switching Characteristics***.

Daisy Chain

Multiple FPGAs in Slave Serial mode can be daisy-chained for configuration from a single source. After an FPGA is configured, data for the next device is sent to the DOUT pin. Data on the DOUT pin changes on the rising edge of CCLK. Note that DOUT changes on the falling edge of CCLK for some Xilinx families but mixed daisy chains are allowed. Configuration must be delayed until $\overline{\text{INIT}}$ pins of all daisy-chained FPGAs are High. For more information, see **Start-up**, page 14.



Notes:
1. If the DriveDone configuration option is not active for any of the FPGAs, pull up DONE with a 3.3KΩ resistor or lower.

Figure 17: **Master/Slave Serial Configuration Circuit Diagram**

Master Serial Mode

In Master Serial mode, the CCLK output of the FPGA drives a Xilinx PROM, which feeds a serial stream of configuration data to the FPGA's DIN input. Figure 17 shows a Master Serial FPGA configuring a Slave Serial FPGA from a PROM. A Spartan-IIE device in Master Serial mode should be connected as shown for the device on the left side. Master Serial mode is selected by a <00x> on the mode pins (M0, M1, M2). The PROM RESET pin is driven by $\overline{\text{INIT}}$, and the CE input is driven by DONE. For more information on serial PROMs, see the Xilinx Configuration PROM data sheets at:

http://www.xilinx.com/xlnx/xweb/xil_publications_index.jsp.

The interface is identical to the slave serial mode except that an oscillator internal to the FPGA is used to generate the configuration clock (CCLK). Any of a number of different frequencies ranging from 4 to 60 MHz can be set using the ConfigRate option in the Xilinx development software. When selecting a CCLK frequency, ensure that the serial PROM and any daisy-chained FPGAs are fast enough to support the clock rate. On power-up, while the first 60 bytes of the configuration data are being loaded, the CCLK frequency is always 2.5 MHz. This frequency is used until the ConfigRate bits, part of the configuration file, have been loaded into the FPGA, at which point the frequency changes to the selected ConfigRate. Unless a different frequency is specified in the design, the default ConfigRate is 4 MHz.

The FPGA accepts one bit of configuration data on each rising CCLK edge. After the FPGA has been loaded, the data for the next device in a daisy-chain is presented on the DOUT pin after the rising CCLK edge. The timing for Master Serial mode is shown in ***Spartan-IIE 1.8V FPGA Family: DC and Switching Characteristics***.

Slave Parallel Mode (SelectMAP)

The Slave Parallel mode, also known as SelectMAP, is the fastest configuration option. Byte-wide data is written into the FPGA on the D0-D7 pins. Note that D0 is the MSB of each byte for configuration. A BUSY flag is provided for controlling the flow of data at a clock frequency above 50 MHz.

Figure 18, page 18 shows the connections for two Spartan-IIE devices using the Slave Parallel mode. Slave Parallel mode is selected by a <011> on the mode pins (M0, M1, M2).

The agent controlling configuration is not shown. Typically, a processor, a microcontroller, or CPLD controls the Slave Parallel interface. The controlling agent provides byte-wide configuration data, CCLK, a Chip Select ($\overline{\text{CS}}$) signal and a Write signal ($\overline{\text{WRITE}}$). If BUSY is asserted (High) by the FPGA, the data must be held until BUSY goes Low.

After configuration, the pins of the Slave Parallel port (D0-D7) can be used as additional user I/O. Alternatively, the port may be retained to permit high-speed 8-bit readback. Then data can be read by deasserting $\overline{\text{WRITE}}$. If retention is selected, prohibit the D0-D7 pins from being used as user I/O. See **Readback**, page 19.

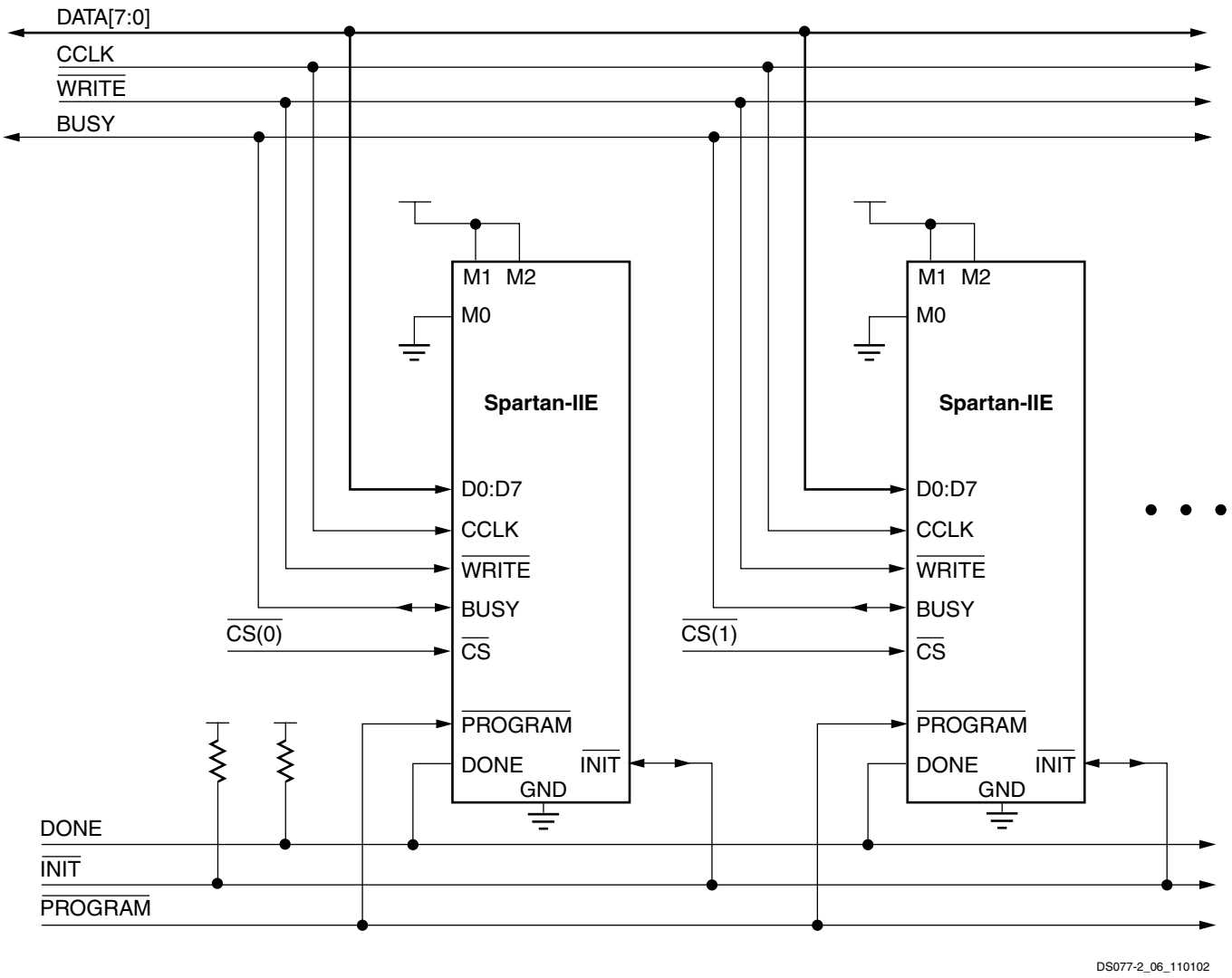


Figure 18: **Slave Parallel Configuration Circuit Diagram**

Multiple Spartan-IIE FPGAs can be configured using the Slave Parallel mode, and be made to start-up simultaneously. To configure multiple devices in this way, wire the individual CCLK, Data, WRITE, and BUSY pins of all the devices in parallel. The individual devices are loaded separately by asserting the CS pin of each device in turn and writing the appropriate data. Sync-to-DONE start-up timing is used to ensure that the start-up sequence does not begin until all the FPGAs have been loaded. See **Start-up**, page 14.

Write

When using the Slave Parallel Mode, write operations send packets of byte-wide configuration data into the FPGA. Figure 19, page 19 shows a flowchart of the write sequence used to load data into the Spartan-IIE FPGA. This is an expansion of the "Load Configuration Data Frames" block in Figure 14, page 14.

The timing for Slave Parallel mode is shown in ***Spartan-IIE 1.8V FPGA Family: DC and Switching Characteristics***.

For the present example, the user holds WRITE and CS Low throughout the sequence of write operations. Note that when CS is asserted on successive CCLKs, WRITE must remain either asserted or deasserted. Otherwise an abort will be initiated, as in the next section.

1. Drive data onto D0-D7. Note that to avoid contention, the data source should not be enabled while CS is Low and WRITE is High. Similarly, while WRITE is High, no more than one device's CS should be asserted.
2. On the rising edge of CCLK: If BUSY is Low, the data is accepted on this clock. If BUSY is High (from a previous write), the data is not accepted. Acceptance will instead occur on the first clock after BUSY goes Low, and the data must be held until this happens.
3. Repeat steps 1 and 2 until all the data has been sent.
4. Deassert CS and WRITE.

If CCLK is slower than F_{CCNH}, the FPGA will never assert BUSY. In this case, the above handshake is unnecessary, and data can simply be entered into the FPGA every CCLK cycle.

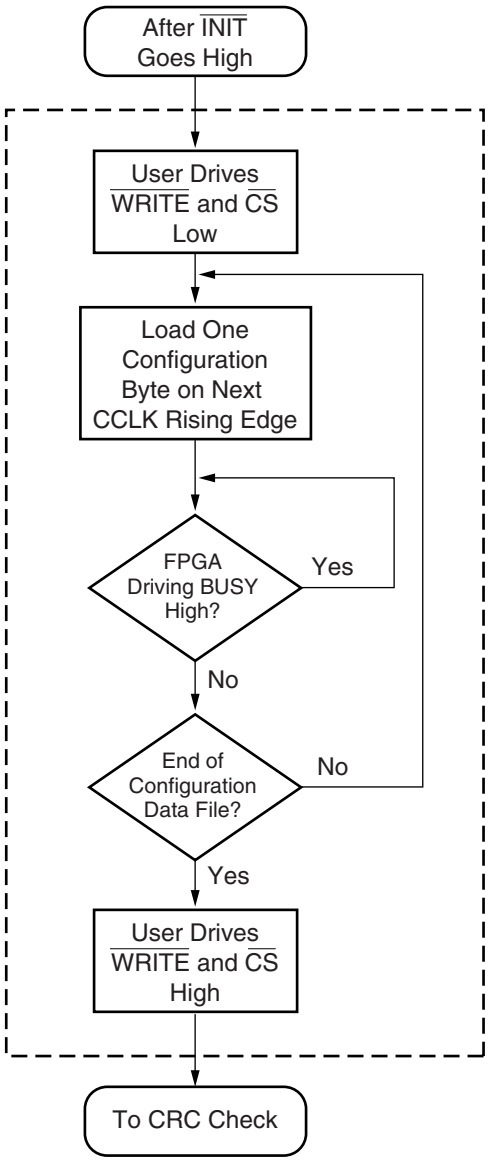


Figure 19: **Loading Configuration Data for the Slave Parallel Mode**

A configuration packet does not have to be written in one continuous stretch, rather it can be split into many write sequences. Each sequence would involve assertion of $\overline{CS}$.

In applications where multiple clock cycles may be required to access the configuration data before each byte can be loaded into the Slave Parallel interface, a new byte of data may not be ready for each consecutive CCLK edge. In such a case the $\overline{CS}$ signal may be deasserted until the next byte is valid on D0-D7. While $\overline{CS}$ is High, the Slave Parallel interface does not expect any data and ignores all CCLK transitions. However, to avoid aborting configuration, $\overline{WRITE}$ must continue to be asserted while $\overline{CS}$ is asserted during CCLK transitions.

Abort

To abort configuration during a write sequence, deassert $\overline{WRITE}$ while holding $\overline{CS}$ Low. The abort operation is initiated at the rising edge of CCLK. The device will remain BUSY until the aborted operation is complete. After aborting configuration, data is assumed to be unaligned to word boundaries and the FPGA requires a new synchronization word prior to accepting any new packets.

Boundary-Scan Configuration Mode

In the boundary-scan mode, no nondedicated pins are required, configuration being done entirely through the IEEE 1149.1 Test Access Port (TAP).

Configuration through the TAP uses the special CFG_IN instruction. This instruction allows data input on TDI to be converted into data packets for the internal configuration bus.

The following steps are required to configure the FPGA through the boundary-scan port.

1. Load the CFG_IN instruction into the boundary-scan instruction register (IR)
2. Enter the Shift-DR (SDR) state
3. Shift a standard configuration bitstream into TDI
4. Return to Run-Test-Idle (RTI)
5. Load the JSTART instruction into IR
6. Enter the SDR state
7. Clock TCK (if selected) through the startup sequence (the length is programmable)
8. Return to RTI

Configuration and readback via the TAP is always available. The boundary-scan mode simply locks out the other modes. The boundary-scan mode is selected by a <10x> on the mode pins (M0, M1, M2). Note that the $\overline{PROGRAM}$ pin must be pulled High prior to reconfiguration. A Low on the $\overline{PROGRAM}$ pin resets the TAP controller and no boundary scan operations can be performed. See Xilinx Application Note **XAPP188** for more information on boundary-scan configuration.

Readback

The configuration data stored in the Spartan-IIE configuration memory can be read back for verification. Along with the configuration data it is possible to read back the contents of all flip-flops/latches, LUT RAMs, and block RAMs. This capability is used for real-time debugging.

For more detailed information see Xilinx Application Note **XAPP176**, *Spartan-II FPGA Series Configuration and Readback*.

Revision History

Version No.	Date	Description
1.0	11/15/01	Initial Xilinx release.
2.0	11/18/02	Added XC2S400E and XC2S600E. Removed Preliminary designation. Clarified details of I/O standards, boundary scan, and configuration.
2.1	07/09/03	Added hot swap description (see **Hot Swap, Hot Insertion, Hot Socketing Support**). Added Table 7 containing JTAG IDCODE values. Clarified configuration PROM support.

The Spartan-IIE Family Data Sheet

DS077-1, ***Spartan-IIE 1.8V FPGA Family: Introduction and Ordering Information*** (Module 1)

DS077-2, ***Spartan-IIE 1.8V FPGA Family: Functional Description*** (Module 2)

DS077-3, ***Spartan-IIE 1.8V FPGA Family: DC and Switching Characteristics*** (Module 3)

DS077-4, ***Spartan-IIE 1.8V FPGA Family: Pinout Tables*** (Module 4)

Spartan-IIE 1.8V FPGA Family: DC and Switching Characteristics

DS077-3 (v2.1) July 9, 2003 **Product Specification**

Definition of Terms

In this document, some specifications may be designated as Advance or Preliminary. These designations are based on the more detailed timing information used by the development system and reported in the output files. These terms are defined as follows:

Advance: Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or families. Values are subject to change. Use as estimates, not for production.

Preliminary: Based on characterization. Further changes are not expected.

Except for pin-to-pin input and output parameters, the AC parameter delay specifications included in this document are derived from measuring internal test patterns. All specifications are representative of worst-case supply voltage and junction temperature conditions. The parameters included are common to popular designs and typical applications. All specifications are subject to change without notice.

DC Specifications

Absolute Maximum Ratings(1)

Symbol	Description	Min	Max	Units
V_{CCINT}	Supply voltage relative to GND	–0.5	2.0	V
V_{CCO}	Supply voltage relative to GND	–0.5	4.0	V
V_{REF}	Input reference voltage	–0.5	4.0	V
V_{IN}	Input voltage relative to GND(2,3)	–0.5	4.0	V
V_{TS}	Voltage applied to 3-state output(3)	–0.5	4.0	V
T_{STG}	Storage temperature (ambient)	–65	+150	°C
T_J	Junction temperature	-	+125	°C

Notes:
1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.
2. V_{IN} should not exceed V_{CCO} by more than 3.6V over extended periods of time (e.g., longer than a day).
3. Maximum DC overshoot must be limited to either V_{CCO} + 0.5V or 10 mA, and undershoot must be limited to –0.5V or 10 mA, whichever is easier to achieve. The Maximum AC conditions are as follows: The device pins may undershoot to –2.0V or overshoot to V_{CCO} + 2.0V, provided this over/undershoot lasts no more than 11 ns with a forcing current no greater than 100 mA.
4. For soldering guidelines, see the Packaging Information on the Xilinx website.

Recommended Operating Conditions

Symbol	Description		Min	Max	Units
T_J	Junction temperature	Commercial	0	85	°C
		Industrial	–40	100	°C
V_{CCINT}	Supply voltage relative to GND(1)	Commercial	1.8 – 5%	1.8 + 5%	V
		Industrial	1.8 – 5%	1.8 + 5%	V
V_{CCO}	Supply voltage relative to GND(2)	Commercial	1.2	3.6	V
		Industrial	1.2	3.6	V
T_{IN}	Input signal transition time(3)		-	250	ns

Notes:
1. Functional operation is guaranteed down to a minimum V_{CCINT} of 1.62V (Nominal V_{CCINT} –10%). For every 50 mV reduction in V_{CCINT} below 1.71V (nominal V_{CCINT} –5%), all delay parameters increase by approximately 3%.
2. Minimum and maximum values for V_{CCO} vary according to the I/O standard selected.
3. Input and output measurement threshold is ~50% of V_{CCO}.

DC Characteristics Over Operating Conditions

Symbol	Description			Min	Typ	Max	Units
V_{DRINT}	Data retention V_{CCINT} voltage (below which configuration data may be lost)			1.5	-	-	V
V_{DRIO}	Data retention V_{CCO} voltage (below which configuration data may be lost)			1.2	-	-	V
I_{CCINTQ}	Quiescent V_{CCINT} supply current(1)	XC2S50E	Commercial	-	10	200	mA
			Industrial	-	10	200	mA
		XC2S100E	Commercial	-	10	200	mA
			Industrial	-	10	200	mA
		XC2S150E	Commercial	-	10	300	mA
			Industrial	-	10	300	mA
		XC2S200E	Commercial	-	10	300	mA
			Industrial	-	10	300	mA
		XC2S300E	Commercial	-	12	300	mA
			Industrial	-	12	300	mA
		XC2S400E	Commercial	-	15	300	mA
			Industrial	-	15	300	mA
		XC2S600E	Commercial	-	15	400	mA
			Industrial	-	15	400	mA
I_{CCOQ}	Quiescent V_{CCO} supply current(1)			-	-	2	mA
I_{REF}	V_{REF} current per V_{REF} pin			-	-	20	µA
I_L	Input or output leakage current per pin			–10	-	+10	µA
C_{IN}	Input capacitance (sample tested)	TQ, PQ, FG, FT packages		-	-	8	pF
I_{RPU}	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 3.3V (sample tested)(2)			-	-	0.25	mA
I_{RPD}	Pad pull-down (when selected) @ V_{IN} = 3.6V (sample tested)(2)			-	-	0.25	mA

Notes:
1. With no output current loads, no active input pull-up resistors, all I/O pins 3-stated and floating.
2. Internal pull-up and pull-down resistors guarantee valid logic levels at unconnected input pins. These pull-up and pull-down resistors do not provide valid logic levels when input pins are connected to other circuits.

Power-On Requirements

Spartan™-IIE FPGAs require that a minimum supply current I_{CCPO} be provided to the V_{CCINT} lines for a successful power-on. If more current is available, the FPGA can consume more than I_{CCPO} min., though this cannot adversely affect reliability.

A maximum limit for I_{CCPO} is not specified. Be careful when using foldback/crowbar supplies and fuses. It is possible to control the magnitude of I_{CCPO} by limiting the supply current available to the FPGA. A current limit below the trip level will avoid inadvertently activating over-current protection circuits.

Symbol	Description				Min(1)	Typ	Max	Units
I_{CCPO}	Total V_{CCINT} supply current required during power-on	Commercial	XC2S50E - XC2S300E	After PCN(2)	300	-	-	mA
				Before PCN(2)	500	-	-	mA
			XC2S400E - XC2S600E		500	-	-	mA
		Industrial	XC2S50E - XC2S300E	After PCN(2)	500	-	-	mA
				Before PCN(2)	2	-	-	A
			XC2S400E - XC2S600E		700	-	-	mA
T_{CCPO}	V_{CCINT}(3,4) ramp time		After PCN(2)		500	-	-	µs
			Before PCN(2)		2	-	50	ms
I_{HSPO}	AC current per pin during power-on in hot-swap applications when $V_{IN} > V_{CCO} + 0.4V$; duration < 10ns		After PCN(2)		-	±60	-	µA

Notes:
1. The I_{CCPO} requirement applies for a brief time (commonly only a few milliseconds) when V_{CCINT} ramps from 0 to 1.8V.
2. Devices built after the Product Change Notice PCN 2002-05 (see http://www.xilinx.com/bvdocs/notifications/pcn2002-05.pdf) have improved power-on requirements. Devices after the PCN have a 'T' preceding the date code as referenced in the PCN. Note that the XC2S150E, XC2S400E, and XC2S600E always have this mark. Devices before the PCN have an 'S' preceding the date code. Note that devices before the PCN are measured with V_{CCINT} and V_{CCO} powering up simultaneously.
3. The ramp time is measured from GND to 1.8V on a fully loaded board.
4. V_{CCINT} must not dip in the negative direction during power on.
5. I/Os are not guaranteed to be disabled until V_{CCINT} is applied.
6. For more information on designing to meet the power-on specifications, refer to the application note **XAPP450 "Power-On Current Requirements for the Spartan-II and Spartan-IIE Families"**.

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for V_{OL} and V_{OH} are guaranteed output voltages over the recommended operating conditions. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at minimum V_{CCO} with the respective I_{OL} and I_{OH} currents shown. Other standards are sample tested.

Input/Output Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
LVTTL(1)	–0.5	0.8	2.0	3.6	0.4	2.4	24	–24
LVCMOS2	–0.5	0.7	1.7	2.7	0.4	1.9	12	–12
LVCMOS18	–0.5	35% V_{CCO}	65% V_{CCO}	1.95	0.4	V_{CCO} – 0.4	8	–8
PCI, 3.3V	–0.5	30% V_{CCO}	50% V_{CCO}	V_{CCO} + 0.5	10% V_{CCO}	90% V_{CCO}	Note (2)	Note (2)
GTL	–0.5	V_{REF} – 0.05	V_{REF} + 0.05	3.6	0.4	-	40	-
GTL+	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.6	-	36	-
HSTL I	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} – 0.4	8	–8

Input/Output Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
HSTL III	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} – 0.4	24	–8
HSTL IV	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} – 0.4	48	–8
SSTL3 I	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.6	V_{REF} + 0.6	8	–8
SSTL3 II	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.8	V_{REF} + 0.8	16	–16
SSTL2 I	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.61	V_{REF} + 0.61	7.6	–7.6
SSTL2 II	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.8	V_{REF} + 0.8	15.2	–15.2
CTT	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.4	V_{REF} + 0.4	8	–8
AGP	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	10% V_{CCO}	90% V_{CCO}	Note (2)	Note (2)

Notes:
1. V_{OL} and V_{OH} for lower drive currents are sample tested.
2. Tested according to the relevant specifications.

LVDS DC Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{CCO}	Supply voltage		2.375	2.5	2.625	V
V_{OH}	Output High voltage for Q and $\overline{Q}$	R_T = 100Ω across Q and $\overline{Q}$ signals	1.25	1.425	1.6	V
V_{OL}	Output Low voltage for Q and $\overline{Q}$	R_T = 100Ω across Q and $\overline{Q}$ signals	0.9	1.075	1.25	V
V_{ODIFF}	Differential output voltage (Q – $\overline{Q}$), Q = High or ($\overline{Q}$ – Q), $\overline{Q}$ = High	R_T = 100Ω across Q and $\overline{Q}$ signals	250	350	450	mV
V_{OCM}	Output common-mode voltage	R_T = 100Ω across Q and $\overline{Q}$ signals	1.125	1.25	1.375	V
V_{IDIFF}	Differential input voltage (Q – $\overline{Q}$), Q = High or ($\overline{Q}$ – Q), $\overline{Q}$ = High	Common-mode input voltage = 1.25 V	100	350	-	mV
V_{ICM}	Input common-mode voltage	Differential input voltage = ±350 mV	0.2	1.25	2.2	V

LVPECL DC Specifications

These values are valid at the output of the source termination pack shown under LVPECL, with a 100Ω differential load only. The V_{OH} levels are 200 mV below standard LVPECL levels and are compatible with devices tolerant of lower common-mode ranges. The following table summarizes the DC output specifications of LVPECL.

DC Parameter	Min	Max	Min	Max	Min	Max	Units
V_{CCO}	3.0		3.3		3.6		V
V_{OH}	1.8	2.11	1.92	2.28	2.13	2.41	V
V_{OL}	0.96	1.27	1.06	1.43	1.30	1.57	V
V_{IH}	1.49	2.72	1.49	2.72	1.49	2.72	V
V_{IL}	0.86	2.125	0.86	2.125	0.86	2.125	V
Differential input voltage	0.3	-	0.3	-	0.3	-	V

Switching Characteristics

Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRACE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan-IIE devices unless otherwise noted.

Global Clock Input to Output Delay for LVTTL, *with* DLL (Pin-to-Pin)(1)

Symbol	Description	Speed Grade			Units
		All	-7	-6	
		Min	Max	Max	
$T_{ICKOFDLL}$	LVTTL global clock input to output delay using output flip-flop for LVTTL, 12 mA, fast slew rate, *with* DLL.	1.0	3.1	3.1	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 50% V_{CC} threshold with 35 pF external capacitive load for LVTTL. The 35 pF load does not apply to the Min values. For other I/O standards and different loads, see the tables **Constants for Calculating TIOOP** and **Delay Measurement Methodology**, page 11.
3. DLL output jitter is already included in the timing calculation.
4. For data *output* with different standards, adjust delays with the values shown in **IOB Output Delay Adjustments for Different Standards(1)**, page 10. For a global clock input with standards other than LVTTL, adjust delays with values from the **I/O Standard Global Clock Input Adjustments**, page 12.

Global Clock Input to Output Delay for LVTTL, *without* DLL (Pin-to-Pin)(1)

Symbol	Description	Device	Speed Grade			Units
			All	-7	-6	
			Min	Max	Max	
T_{ICKOF}	LVTTL global clock input to output delay using output flip-flop for LVTTL, 12 mA, fast slew rate, *without* DLL.	XC2S50E	1.5	4.4	4.6	ns
		XC2S100E	1.5	4.4	4.6	ns
		XC2S150E	1.5	4.5	4.7	ns
		XC2S200E	1.5	4.5	4.7	ns
		XC2S300E	1.5	4.5	4.7	ns
		XC2S400E	1.5	4.6	4.8	ns
		XC2S600E	1.6	4.7	4.9	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 50% V_{CC} threshold with 35 pF external capacitive load for LVTTL. The 35 pF load does not apply to the Min values. For other I/O standards and different loads, see the tables **Constants for Calculating TIOOP** and **Delay Measurement Methodology**, page 11.
3. For data *output* with different standards, adjust delays with the values shown in **IOB Output Delay Adjustments for Different Standards(1)**, page 10. For a global clock input with standards other than LVTTL, adjust delays with values from the **I/O Standard Global Clock Input Adjustments**, page 12.

Global Clock Setup and Hold for LVTTL Standard, *with* DLL (Pin-to-Pin)

Symbol	Description	Speed Grade		Units
		-7	-6	
		Min	Min	
T_{PSDLL} / T_{PHDLL}	Input setup and hold time relative to global clock input signal for LVTTL standard, no delay, IFF,(1) *with* DLL	1.6 / 0	1.7 / 0	ns

Notes:
1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
3. DLL output jitter is already included in the timing calculation.
4. For data input with different standards, adjust the setup time delay by the values shown in **IOB Input Delay Adjustments for Different Standards, page 8**. For a global clock input with standards other than LVTTL, adjust delays with values from the **I/O Standard Global Clock Input Adjustments, page 12**.
5. A zero hold time listing indicates no hold time or a negative hold time.

Global Clock Setup and Hold for LVTTL Standard, *without* DLL (Pin-to-Pin)

Symbol	Description	Device	Speed Grade		Units
			-7	-6	
			Min	Min	
T_{PSFD} / T_{PHFD}	Input setup and hold time relative to global clock input signal for LVTTL standard, with delay, IFF,(1) *without* DLL	XC2S50E	1.8 / 0	1.8 / 0	ns
		XC2S100E	1.8 / 0	1.8 / 0	ns
		XC2S150E	1.9 / 0	1.9 / 0	ns
		XC2S200E	1.9 / 0	1.9 / 0	ns
		XC2S300E	2.0 / 0	2.0 / 0	ns
		XC2S400E	2.0 / 0	2.0 / 0	ns
		XC2S600E	2.1 / 0	2.1 / 0	ns

Notes:
1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
3. For data input with different standards, adjust the setup time delay by the values shown in **IOB Input Delay Adjustments for Different Standards, page 8**. For a global clock input with standards other than LVTTL, adjust delays with values from the **I/O Standard Global Clock Input Adjustments, page 12**.

IOB Input Switching Characteristics(1)

Input delays associated with the pad are specified for LVTTL levels. For other standards, adjust the delays with the values shown in **IOB Input Delay Adjustments for Different Standards**, page 8.

Symbol	Description	Device	Speed Grade				Units
			-7		-6		
			Min	Max	Min	Max	
Propagation Delays							
T_{IOPI}	Pad to I output, no delay	All	0.4	0.8	0.4	0.8	ns
T_{IOPID}	Pad to I output, with delay	All	0.5	1.0	0.5	1.0	ns
T_{IOPLI}	Pad to output IQ via transparent latch, no delay	All	0.7	1.5	0.7	1.6	ns
T_{IOPLID}	Pad to output IQ via transparent latch, with delay	XC2S50E	1.3	3.0	1.3	3.1	ns
		XC2S100E	1.3	3.0	1.3	3.1	ns
		XC2S150E	1.3	3.2	1.3	3.3	ns
		XC2S200E	1.3	3.2	1.3	3.3	ns
		XC2S300E	1.3	3.2	1.3	3.3	ns
		XC2S400E	1.4	3.2	1.4	3.4	ns
		XC2S600E	1.5	3.5	1.5	3.7	ns
Sequential Delays							
T_{IOCKIQ}	Clock CLK to output IQ	All	0.1	0.7	0.1	0.7	ns
Setup/Hold Times with Respect to Clock CLK							
T_{IOPICK} / T_{IOICKP}	Pad, no delay	All	1.4 / 0	-	1.5 / 0	-	ns
$T_{IOPICKD}$ / $T_{IOICKPD}$	Pad, with delay	XC2S50E	2.9 / 0	-	2.9 / 0	-	ns
		XC2S100E	2.9 / 0	-	2.9 / 0	-	ns
		XC2S150E	3.1 / 0	-	3.1 / 0	-	ns
		XC2S200E	3.1 / 0	-	3.1 / 0	-	ns
		XC2S300E	3.1 / 0	-	3.1 / 0	-	ns
		XC2S400E	3.2 / 0	-	3.2 / 0	-	ns
		XC2S600E	3.5 / 0	-	3.5 / 0	-	ns
$T_{IOICECK}$ / $T_{IOCKICE}$	ICE input	All	0.7 / 0.01	-	0.7 / 0.01	-	ns
Set/Reset Delays							
$T_{IOSRCKI}$	SR input (IFF, synchronous)	All	0.9	-	1.0	-	ns
T_{IOSRIQ}	SR input to IQ (asynchronous)	All	0.5	1.2	0.5	1.4	ns
T_{GSRQ}	GSR to output IQ	All	3.8	8.5	3.8	9.7	ns

Notes:
1. Input timing for LVTTL is measured at 1.4V. For other I/O standards, see the table **Delay Measurement Methodology**, page 11.

IOB Input Delay Adjustments for Different Standards

Input delays associated with the pad are specified for LVTTL. For other standards, adjust the delays by the values shown. A delay adjusted in this way constitutes a worst-case limit.

Symbol	Description	Standard	Speed Grade		Units
			-7	-6	
Data Input Delay Adjustments					
T_{ILVTTL}	Standard-specific data input delay adjustments	LVTTL	0	0	ns
$T_{ILVCMOS2}$		LVCMOS2	0	0	ns
$T_{ILVCMOS18}$		LVCMOS18	0.20	0.20	ns
T_{ILVDS}		LVDS	0.15	0.15	ns
$T_{ILVPECL}$		LVPECL	0.15	0.15	ns
T_{IPCI33_3}		PCI, 33 MHz, 3.3V	0.08	0.08	ns
T_{IPCI66_3}		PCI, 66 MHz, 3.3V	–0.11	–0.11	ns
T_{IGTL}		GTL	0.14	0.14	ns
T_{IGTLP}		GTL+	0.14	0.14	ns
T_{IHSTL}		HSTL	0.04	0.04	ns
T_{ISSTL2}		SSTL2	0.04	0.04	ns
T_{ISSTL3}		SSTL3	0.04	0.04	ns
T_{ICTT}		CTT	0.10	0.10	ns
T_{IAGP}		AGP	0.04	0.04	ns

IOB Output Switching Characteristics

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays with the values shown in **IOB Output Delay Adjustments for Different Standards(1)**, page 10.

Symbol	Description	Speed Grade				Units
		-7		-6		
		Min	Max	Min	Max	
Propagation Delays						
T_{IOOP}	O input to pad	1.0	2.7	1.0	2.9	ns
T_{IOOLP}	O input to pad via transparent latch	1.2	3.1	1.2	3.4	ns
3-state Delays						
T_{IOTHZ}	T input to pad high impedance(1)	0.7	1.7	0.7	1.9	ns
T_{IOTON}	T input to valid data on pad	1.1	2.9	1.1	3.1	ns
$T_{IOTLPHZ}$	T input to pad high impedance via transparent latch(1)	0.8	2.0	0.8	2.2	ns
$T_{IOTLPON}$	T input to valid data on pad via transparent latch	1.2	3.2	1.2	3.4	ns
T_{GTS}	GTS to pad high impedance(1)	1.9	4.6	1.9	4.9	ns
Sequential Delays						
T_{IOCKP}	Clock CLK to pad	0.9	2.8	0.9	2.9	ns
T_{IOCKHZ}	Clock CLK to pad high impedance (synchronous)(1)	0.7	2.0	0.7	2.2	ns
T_{IOCKON}	Clock CLK to valid data on pad (synchronous)	1.1	3.2	1.1	3.4	ns
Setup/Hold Times with Respect to Clock CLK						
T_{IOOCK} / T_{IOCKO}	O input	1.0 / 0	-	1.1 / 0	-	ns
$T_{IOOCECK}$ / $T_{IOCKOCE}$	OCE input	0.7 / 0	-	0.7 / 0	-	ns
$T_{IOSRCKO}$ / $T_{IOCKOSR}$	SR input (OFF)	0.9 / 0	-	1.0 / 0	-	ns
T_{IOTCK} / T_{IOCKT}	3-state setup times, T input	0.6 / 0	-	0.7 / 0	-	ns
$T_{IOTCECK}$ / $T_{IOCKTCE}$	3-state setup times, TCE input	0.6 / 0	-	0.8 / 0	-	ns
$T_{IOSRCKT}$ / $T_{IOCKTSR}$	3-state setup times, SR input (TFF)	0.9 / 0	-	1.0 / 0	-	ns
Set/Reset Delays						
T_{IOSRP}	SR input to pad (asynchronous)	1.2	3.3	1.2	3.5	ns
T_{IOSRHZ}	SR input to pad high impedance (asynchronous)(1)	1.0	2.4	1.0	2.7	ns
T_{IOSRON}	SR input to valid data on pad (asynchronous)	1.4	3.7	1.4	3.9	ns
T_{IOGSRQ}	GSR to pad	3.8	8.5	3.8	9.7	ns

Notes:
1. Three-state turn-off delays should not be adjusted.

IOB Output Delay Adjustments for Different Standards(1)

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays by the values shown. A delay adjusted in this way constitutes a worst-case limit.

Symbol	Description	Standard	Speed Grade		Units
			-7	-6	
Output Delay Adjustments (Adj)					
T_{OLVTTL_S2}	Standard-specific adjustments for output delays terminating at pads (based on standard capacitive load, C_{SL})	LVTTL, Slow, 2 mA	14.7	14.7	ns
T_{OLVTTL_S4}		4 mA	7.5	7.5	ns
T_{OLVTTL_S6}		6 mA	4.8	4.8	ns
T_{OLVTTL_S8}		8 mA	3.0	3.0	ns
T_{OLVTTL_S12}		12 mA	1.9	1.9	ns
T_{OLVTTL_S16}		16 mA	1.7	1.7	ns
T_{OLVTTL_S24}		24 mA	1.3	1.3	ns
T_{OLVTTL_F2}		LVTTL, Fast, 2 mA	13.1	13.1	ns
T_{OLVTTL_F4}		4 mA	5.3	5.3	ns
T_{OLVTTL_F6}		6 mA	3.1	3.1	ns
T_{OLVTTL_F8}		8 mA	1.0	1.0	ns
T_{OLVTTL_F12}		12 mA	0	0	ns
T_{OLVTTL_F16}		16 mA	–0.05	–0.05	ns
T_{OLVTTL_F24}		24 mA	–0.20	–0.20	ns
$T_{OLVCMOS2}$		LVCMOS2	0.09	0.09	ns
$T_{OLVCMOS18}$		LVCMOS18	0.7	0.7	ns
T_{OLVDS}		LVDS	–1.2	–1.2	ns
$T_{OLVPECL}$		LVPECL	–0.41	–0.41	ns
T_{OPCI33_3}		PCI, 33 MHz, 3.3V	2.3	2.3	ns
T_{OPCI66_3}		PCI, 66 MHz, 3.3V	–0.41	–0.41	ns
T_{OGTL}		GTL	0.49	0.49	ns
T_{OGTLP}		GTL+	0.8	0.8	ns
T_{OHSTL_I}		HSTL I	–0.51	–0.51	ns
T_{OHSTL_III}		HSTL III	–0.91	–0.91	ns
T_{OHSTL_IV}		HSTL IV	–1.01	–1.01	ns
T_{OSSTL2_I}		SSTL2 I	–0.51	–0.51	ns
T_{OSSLT2_II}		SSTL2 II	–0.91	–0.91	ns
T_{OSSTL3_I}		SSTL3 I	–0.51	–0.51	ns
T_{OSSTL3_II}		SSTL3 II	–1.01	–1.01	ns
T_{OCTT}		CTT	–0.61	–0.61	ns
T_{OAGP}		AGP	–0.91	–0.91	ns

Notes:

1. Output timing is measured at 1.4V with 35 pF external capacitive load for LVTTL. For other I/O standards and different loads, see the tables **Constants for Calculating TIOOP** and **Delay Measurement Methodology**, page 11.

Calculation of T_{IOOP} as a Function of Capacitance

T_{IOOP} is the propagation delay from the O Input of the IOB to the pad. The values for T_{IOOP} are based on the standard capacitive load (C_{SL}) for each I/O standard as listed in the table **Constants for Calculating TIOOP**, below.

For other capacitive loads, use the formulas below to calculate an adjusted propagation delay, T_{IOOP1}.

$$T_{IOOP1} = T_{IOOP} + Adj + (C_{LOAD} - C_{SL}) * F_L$$

Where:

- Adj — is selected from **IOB Output Delay Adjustments for Different Standards(1)**, page 10, according to the I/O standard used
- C_{LOAD} — is the capacitive load for the design
- F_L — is the capacitance scaling factor

Delay Measurement Methodology

Standard	V_L[1]	V_H[1]	Meas. Point	V_{REF} Typ[2]
LVTTL	0	3	1.4	-
LVCMOS2	0	2.5	1.125	-
PCI33_3	Per PCI Spec			-
PCI66_3	Per PCI Spec			-
GTL	V_{REF} – 0.2	V_{REF} + 0.2	V_{REF}	0.80
GTL+	V_{REF} – 0.2	V_{REF} + 0.2	V_{REF}	1.0
HSTL Class I	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.75
HSTL Class III	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
HSTL Class IV	V_{REF} – 0.5	V_{REF} + 0.5	V_{REF}	0.90
SSTL3 I and II	V_{REF} – 1.0	V_{REF} + 1.0	V_{REF}	1.5
SSTL2 I and II	V_{REF} – 0.75	V_{REF} + 0.75	V_{REF}	1.25
CTT	V_{REF} – 0.2	V_{REF} + 0.2	V_{REF}	1.5
AGP	V_{REF} – (0.2xV_{CCO})	V_{REF} + (0.2xV_{CCO})	V_{REF}	Per AGP Spec
LVDS	1.2 – 0.125	1.2 + 0.125	1.2	
LVPECL	1.6 – 0.3	1.6 + 0.3	1.6	

Notes:

1. Input waveform switches between V_L and V_H.
2. Measurements are made at V_{REF} Typ, Maximum, and Minimum. Worst-case values are reported.
3. I/O parameter measurements are made with the capacitance values shown in the following table, **Constants for Calculating TIOOP**. Refer to Application Note XAPP179 for appropriate terminations.
4. I/O standard measurements are reflected in the IBIS model information except where the IBIS format precludes it.

Constants for Calculating T_{IOOP}

Standard	C_{SL}[1] (pF)	F_L (ns/pF)
LVTTL Fast Slew Rate, 2 mA drive	35	0.41
LVTTL Fast Slew Rate, 4 mA drive	35	0.20
LVTTL Fast Slew Rate, 6 mA drive	35	0.13
LVTTL Fast Slew Rate, 8 mA drive	35	0.079
LVTTL Fast Slew Rate, 12 mA drive	35	0.044
LVTTL Fast Slew Rate, 16 mA drive	35	0.043
LVTTL Fast Slew Rate, 24 mA drive	35	0.033
LVTTL Slow Slew Rate, 2 mA drive	35	0.41
LVTTL Slow Slew Rate, 4 mA drive	35	0.20
LVTTL Slow Slew Rate, 6 mA drive	35	0.100
LVTTL Slow Slew Rate, 8 mA drive	35	0.086
LVTTL Slow Slew Rate, 12 mA drive	35	0.058
LVTTL Slow Slew Rate, 16 mA drive	35	0.050
LVTTL Slow Slew Rate, 24 mA drive	35	0.048
LVCMOS2	35	0.041
LVCMOS18	35	0.050
PCI 33 MHz 3.3V	10	0.050
PCI 66 MHz 3.3V	10	0.033
GTL	0	0.014
GTL+	0	0.017
HSTL Class I	20	0.022
HSTL Class III	20	0.016
HSTL Class IV	20	0.014
SSTL2 Class I	30	0.028
SSTL2 Class II	30	0.016
SSTL3 Class I	30	0.029
SSTL3 Class II	30	0.016
CTT	20	0.035
AGP	10	0.037

Notes:

1. I/O parameter measurements are made with the capacitance values shown above. Refer to Application Note XAPP179 for appropriate terminations.
2. I/O standard measurements are reflected in the IBIS model information except where the IBIS format precludes it.

Clock Distribution Switching Characteristics

T_{GPIO} is specified for LVTTL levels. For other standards, adjust T_{GPIO} with the values shown in **I/O Standard Global Clock Input Adjustments**.

Symbol	Description	Speed Grade		Units
		-7	-6	
		Max	Max	
GCLK IOB and Buffer				
T_{GPIO}	Global clock pad to output	0.7	0.7	ns
T_{GIO}	Global clock buffer I input to O output	0.45	0.5	ns

I/O Standard Global Clock Input Adjustments

Delays associated with a global clock input pad are specified for LVTTL levels. For other standards, adjust the delays by the values shown. A delay adjusted in this way constitutes a worst-case limit.

Symbol	Description	Standard	Speed Grade		Units
			-7	-6	
Data Input Delay Adjustments					
$T_{GPLVTTL}$	Standard-specific global clock input delay adjustments	LVTTL	0	0	ns
$T_{GPLVCMOS2}$		LVCMOS2	0	0	ns
$T_{GPLVCMOS18}$		LVCMOS18	0.2	0.2	ns
$T_{GPLVCDS}$		LVDS	0.38	0.38	ns
$T_{GPLVPECL}$		LVCPECL	0.38	0.38	ns
$T_{GPPCI33\_3}$		PCI, 33 MHz, 3.3V	0.08	0.08	ns
$T_{GPPCI66\_3}$		PCI, 66 MHz, 3.3V	–0.11	–0.11	ns
T_{GPGTL}		GTL	0.37	0.37	ns
T_{GPGTLP}		GTL+	0.37	0.37	ns
T_{GPHSTL}		HSTL	0.27	0.27	ns
$T_{GPSSTL2}$		SSTL2	0.27	0.27	ns
$T_{GPSSTL3}$		SSTL3	0.27	0.27	ns
T_{GPCTT}		CTT	0.33	0.33	ns
T_{GPAGP}		AGP	0.27	0.27	ns

Notes:
1. Input timing for GPLVTTL is measured at 1.4V. For other I/O standards, see the table **Delay Measurement Methodology**, page 11.

DLL Timing Parameters

Because of the difficulty in directly measuring many internal timing parameters, those parameters are derived from benchmark timing patterns. The following guidelines reflect worst-case values across the recommended operating conditions.

Symbol	Description	F_{CLKIN}	Speed Grade				Units
			-7		-6		
			Min	Max	Min	Max	
$F_{CLKINHF}$	Input clock frequency (CLKDLLHF)	-	60	320	60	275	MHz
$F_{CLKINLF}$	Input clock frequency (CLKDLL)	-	25	160	25	135	MHz
T_{DLLPW}	Input clock pulse width	≥25 MHz	5.0	-	5.0	-	ns
		≥50 MHz	3.0	-	3.0	-	ns
		≥100 MHz	2.4	-	2.4	-	ns
		≥150 MHz	2.0	-	2.0	-	ns
		≥200 MHz	1.8	-	1.8	-	ns
		≥250 MHz	1.5	-	1.5	-	ns
		≥300 MHz	1.3	-	NA	-	

DLL Clock Tolerance, Jitter, and Phase Information

All DLL output jitter and phase specifications were determined through statistical measurement at the package pins using a clock mirror configuration and matched drivers.

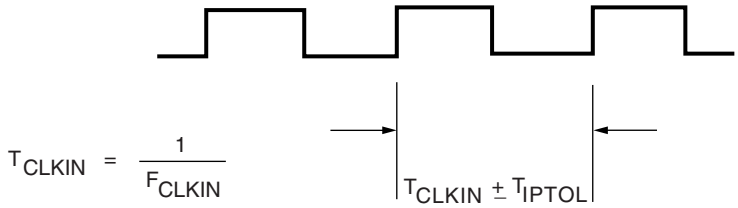
Figure 1, page 14, provides definitions for various parameters in the table below.

Symbol	Description	F_{CLKIN}	CLKDLLHF		CLKDLL		Units
			Min	Max	Min	Max	
T_{IPTOL}	Input clock period tolerance		-	1.0	-	1.0	ns
T_{IJITCC}	Input clock jitter tolerance (cycle-to-cycle)		-	±150	-	±300	ps
T_{LOCK}	Time required for DLL to acquire lock(1)	> 60 MHz	-	20	-	20	µs
		50-60 MHz	-	-	-	25	µs
		40-50 MHz	-	-	-	50	µs
		30-40 MHz	-	-	-	90	µs
		25-30 MHz	-	-	-	120	µs
T_{OJITCC}	Output jitter (cycle-to-cycle) for any DLL clock output(2)		-	±60	-	±60	ps
T_{PHIO}	Phase offset between CLKIN and CLKO(3)		-	±100	-	±100	ps
T_{PHOO}	Phase offset between clock outputs on the DLL(4)		-	±140	-	±140	ps
T_{PHIOM}	Phase difference between CLKIN and CLKO(5)		-	±160	-	±160	ps
T_{PHOOM}	Phase difference between clock outputs on the DLL(6)		-	±200	-	±200	ps

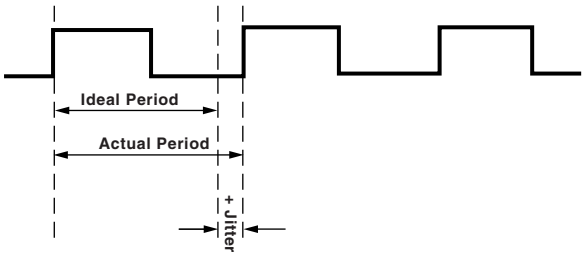
Notes:

1. Commercial operating conditions. Add 30% for Industrial operating conditions.
2. **Output Jitter** is cycle-to-cycle jitter measured on the DLL output clock, *excluding* input clock jitter.
3. **Phase Offset between CLKIN and CLKO** is the worst-case fixed time difference between rising edges of CLKIN and CLKO, *excluding* output jitter and input clock jitter.
4. **Phase Offset between Clock Outputs on the DLL** is the worst-case fixed time difference between rising edges of any two DLL outputs, *excluding* output jitter and input clock jitter.
5. **Maximum Phase Difference between CLKIN and CLKO** is the sum of output jitter and phase offset between CLKIN and CLKO, or the greatest difference between CLKIN and CLKO rising edges due to DLL alone (*excluding* input clock jitter).
6. **Maximum Phase Difference between Clock Outputs on the DLL** is the sum of output jitter and phase offset between any DLL clock outputs, or the greatest difference between any two DLL output rising edges due to DLL alone (*excluding* input clock jitter).

Period Tolerance: the allowed input clock period change in nanoseconds.



Output Jitter: the difference between an ideal reference clock edge and the actual design.



Phase Offset and Maximum Phase Difference

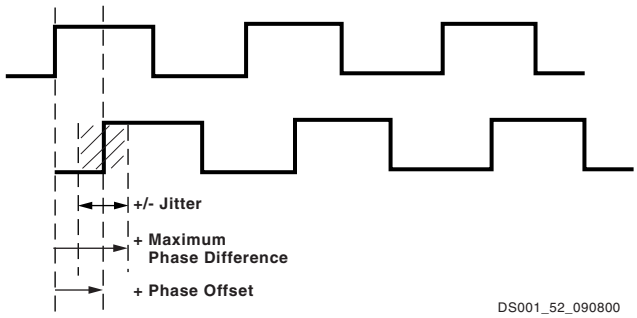


Figure 1: **Period Tolerance and Clock Jitter**

CLB Switching Characteristics

Delays originating at F/G inputs vary slightly according to the input used. The values listed below are worst-case. Precise values are provided by the timing analyzer.

Symbol	Description	Speed Grade				Units
		-7		-6		
		Min	Max	Min	Max	
Combinatorial Delays						
T_{ILO}	4-input function: F/G inputs to X/Y outputs	0.18	0.42	0.18	0.47	ns
T_{IF5}	5-input function: F/G inputs to F5 output	0.3	0.8	0.3	0.9	ns
T_{IF5X}	5-input function: F/G inputs to X output	0.3	0.8	0.3	0.9	ns
T_{IF6Y}	6-input function: F/G inputs to Y output via F6 MUX	0.3	0.9	0.3	1.0	ns
T_{F5INY}	6-input function: F5IN input to Y output	0.04	0.2	0.04	0.22	ns
T_{IFNCTL}	Incremental delay routing through transparent latch to XQ/YQ outputs	-	0.7	-	0.8	ns
T_{BYYB}	BY input to YB output	0.18	0.46	0.18	0.51	ns
Sequential Delays						
T_{CKO}	FF clock CLK to XQ/YQ outputs	0.3	0.9	0.3	1.0	ns
T_{CKLO}	Latch clock CLK to XQ/YQ outputs	0.3	0.9	0.3	1.0	ns
Setup/Hold Times with Respect to Clock CLK						
T_{ICK} / T_{CKI}	4-input function: F/G inputs	1.0 / 0	-	1.1 / 0	-	ns
T_{IF5CK} / T_{CKIF5}	5-input function: F/G inputs	1.4 / 0	-	1.5 / 0	-	ns
T_{F5INCK} / T_{CKF5IN}	6-input function: F5IN input	0.8 / 0	-	0.8 / 0	-	ns
T_{IF6CK} / T_{CKIF6}	6-input function: F/G inputs via F6 MUX	1.5 / 0	-	1.6 / 0	-	ns
T_{DICK} / T_{CKDI}	BX/BY inputs	0.7 / 0	-	0.8 / 0	-	ns
T_{CECK} / T_{CKCE}	CE input	0.7 / 0	-	0.7 / 0	-	ns
T_{RCK} / T_{CKR}	SR/BY inputs (synchronous)	0.52 / 0	-	0.6 / 0	-	ns
Clock CLK						
T_{CH}	Pulse width, High	1.3	-	1.4	-	ns
T_{CL}	Pulse width, Low	1.3	-	1.4	-	ns
Set/Reset						
T_{RPW}	Pulse width, SR/BY inputs	2.1	-	2.4	-	ns
T_{RQ}	Delay from SR/BY inputs to XQ/YQ outputs (asynchronous)	0.3	0.9	0.3	1.0	ns
F_{TOG}	Toggle frequency (for export control)	-	400	-	357	MHz

CLB Arithmetic Switching Characteristics

Setup times not listed explicitly can be approximated by decreasing the combinatorial delays by the setup time adjustment listed. Precise values are provided by the timing analyzer.

Symbol	Description	Speed Grade				Units
		-7		-6		
		Min	Max	Min	Max	
Combinatorial Delays						
T_{OPX}	F operand inputs to X via XOR	-	0.8	-	0.8	ns
T_{OPXB}	F operand input to XB output	-	0.8	-	0.9	ns
T_{OPY}	F operand input to Y via XOR	-	1.4	-	1.5	ns
T_{OPYB}	F operand input to YB output	-	1.1	-	1.3	ns
T_{OPCYF}	F operand input to COUT output	-	0.9	-	1.0	ns
T_{OPGY}	G operand inputs to Y via XOR	-	0.8	-	0.9	ns
T_{OPGYB}	G operand input to YB output	-	1.2	-	1.3	ns
T_{OPCYG}	G operand input to COUT output	-	0.9	-	1.0	ns
T_{BXCY}	BX initialization input to COUT	-	0.51	-	0.6	ns
T_{CINX}	CIN input to X output via XOR	-	0.6	-	0.7	ns
T_{CINXB}	CIN input to XB	-	0.07	-	0.1	ns
T_{CINY}	CIN input to Y via XOR	-	0.7	-	0.7	ns
T_{CINYB}	CIN input to YB	-	0.4	-	0.5	ns
T_{BYP}	CIN input to COUT output	-	0.14	-	0.15	ns
Multiplier Operation						
T_{FANDXB}	F1/2 operand inputs to XB output via AND	-	0.35	-	0.4	ns
T_{FANDYB}	F1/2 operand inputs to YB output via AND	-	0.7	-	0.8	ns
T_{FANDCY}	F1/2 operand inputs to COUT output via AND	-	0.5	-	0.6	ns
T_{GANDYB}	G1/2 operand inputs to YB output via AND	-	0.6	-	0.7	ns
T_{GANDCY}	G1/2 operand inputs to COUT output via AND	-	0.3	-	0.4	ns
Setup/Hold Times with Respect to Clock CLK						
T_{CCKX} / T_{CKCX}	CIN input to FFX	1.2 / 0	-	1.3 / 0	-	ns
T_{CCKY} / T_{CKCY}	CIN input to FFY	1.2 / 0	-	1.3 / 0	-	ns

CLB Distributed RAM Switching Characteristics

Symbol	Description	Speed Grade				Units
		-7		-6		
		Min	Max	Min	Max	
Sequential Delays						
$T_{SHCKO16}$	Clock CLK to X/Y outputs (WE active, 16 x 1 mode)	0.6	1.5	0.6	1.7	ns
$T_{SHCKO32}$	Clock CLK to X/Y outputs (WE active, 32 x 1 mode)	0.8	1.9	0.8	2.1	ns
Setup/Hold Times with Respect to Clock CLK						
T_{AS} / T_{AH}	F/G address inputs	0.42 / 0	-	0.5 / 0	-	ns
T_{DS} / T_{DH}	BX/BY data inputs (DIN)	0.53 / 0	-	0.6 / 0	-	ns
T_{WS} / T_{WH}	CE input (WS)	0.7 / 0	-	0.8 / 0	-	ns
Clock CLK						
T_{WPH}	Pulse width, High	2.1	-	2.4	-	ns
T_{WPL}	Pulse width, Low	2.1	-	2.4	-	ns
T_{WC}	Clock period to meet address write cycle time	4.2	-	4.8	-	ns

CLB Shift Register Switching Characteristics

Symbol	Description	Speed Grade				Units
		-7		-6		
		Min	Max	Min	Max	
Sequential Delays						
T_{REG}	Clock CLK to X/Y outputs	1.2	2.9	1.2	3.2	ns
Setup/Hold Times with Respect to Clock CLK						
T_{SHDICK}	BX/BY data inputs (DIN)	0.53 / 0	-	0.6 / 0	-	ns
T_{SHCECK}	CE input (WS)	0.7 / 0	-	0.8 / 0	-	ns
Clock CLK						
T_{SRPH}	Pulse width, High	2.1	-	2.4	-	ns
T_{SRPL}	Pulse width, Low	2.1	-	2.4	-	ns

Block RAM Switching Characteristics

Symbol	Description	Speed Grade				Units
		-7		-6		
		Min	Max	Min	Max	
Sequential Delays						
T_{BCKO}	Clock CLK to DOUT output	0.6	3.1	0.6	3.5	ns
Setup/Hold Times with Respect to Clock CLK						
T_{BACK} / T_{BCKA}	ADDR inputs	1.0 / 0	-	1.1 / 0	-	ns
T_{BDCK}/ T_{BCKD}	DIN inputs	1.0 / 0	-	1.1 / 0	-	ns
T_{BECK}/ T_{BCKE}	EN inputs	2.2 / 0	-	2.5 / 0	-	ns
T_{BRCK}/ T_{BCKR}	RST input	2.1 / 0	-	2.3 / 0	-	ns
T_{BWCK}/ T_{BCKW}	WEN input	2.0 / 0	-	2.2 / 0	-	ns
Clock CLK						
T_{BPWH}	Pulse width, High	1.4	-	1.5	-	ns
T_{BPWL}	Pulse width, Low	1.4	-	1.5	-	ns
T_{BCCS}	CLKA -> CLKB setup time for different ports	2.7	-	3.0	-	ns

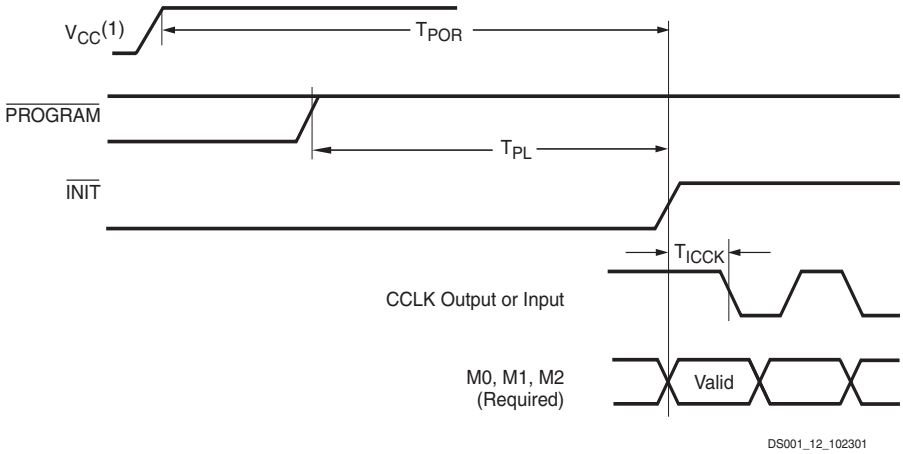
TBUF Switching Characteristics

Symbol	Description	Speed Grade		Units
		-7	-6	
		Max	Max	
T_{IO}	IN input to OUT output	0	0	ns
T_{OFF}	TRI input to OUT output high impedance	0.1	0.11	ns
T_{ON}	TRI input to valid data on OUT output	0.1	0.11	ns

JTAG Test Access Port Switching Characteristics

Symbol	Description	Speed Grade				Units
		-7		-6		
		Min	Max	Min	Max	
Setup/Hold Times with Respect to TCK						
T_{TAPTCK} / T_{TCKTAP}	TMS and TDI setup times and hold times	4.0 / 2.0	-	4.0 / 2.0	-	ns
Sequential Delays						
T_{TCKTDO}	Output delay from clock TCK to output TDO	-	11.0	-	11.0	ns
F_{TCK}	TCK clock frequency	-	33	-	33	MHz

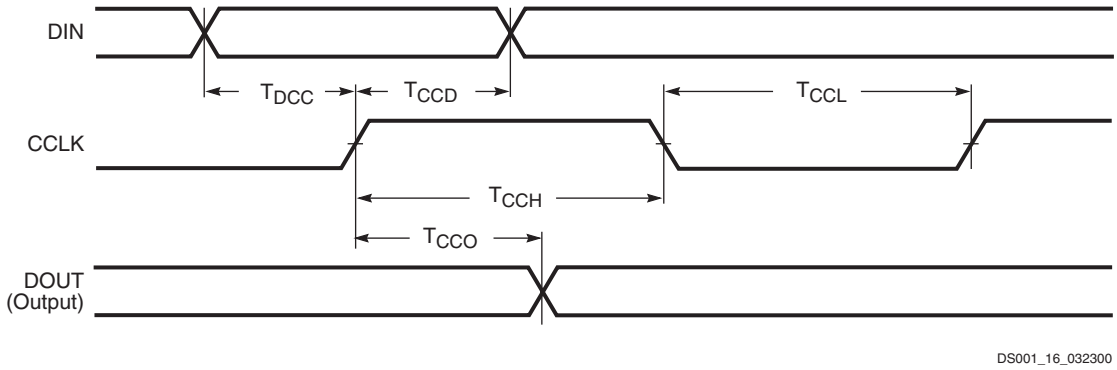
Configuration Switching Characteristics



Symbol	Description	All Devices		Units
		Min	Max	
T_{POR}	Power-on reset	-	2	ms
T_{PL}	Program latency	-	100	µs
T_{ICCK}	CCLK output delay (Master serial mode only)	0.5	4	µs
$T_{PROGRAM}$	Program pulse width	300	-	ns

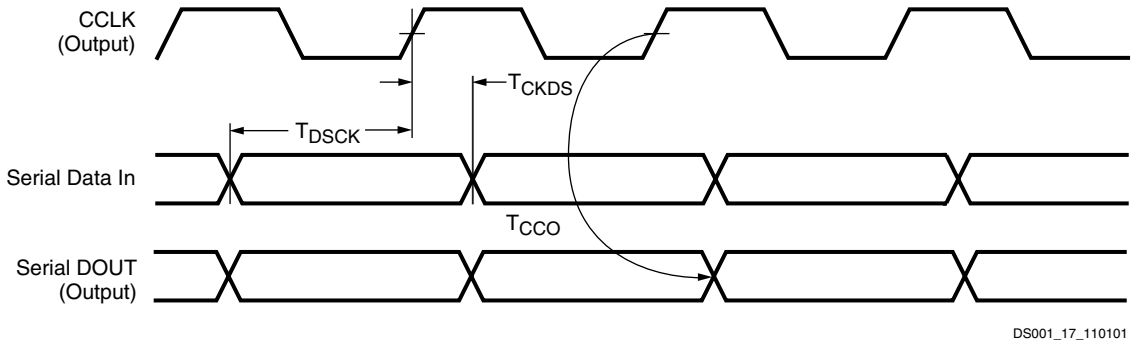
Notes:
1. Before configuration can begin, V_{CCINT} and V_{CCO} Bank 2 must reach the recommended operating voltage.

Figure 2: **Configuration Timing on Power-Up**



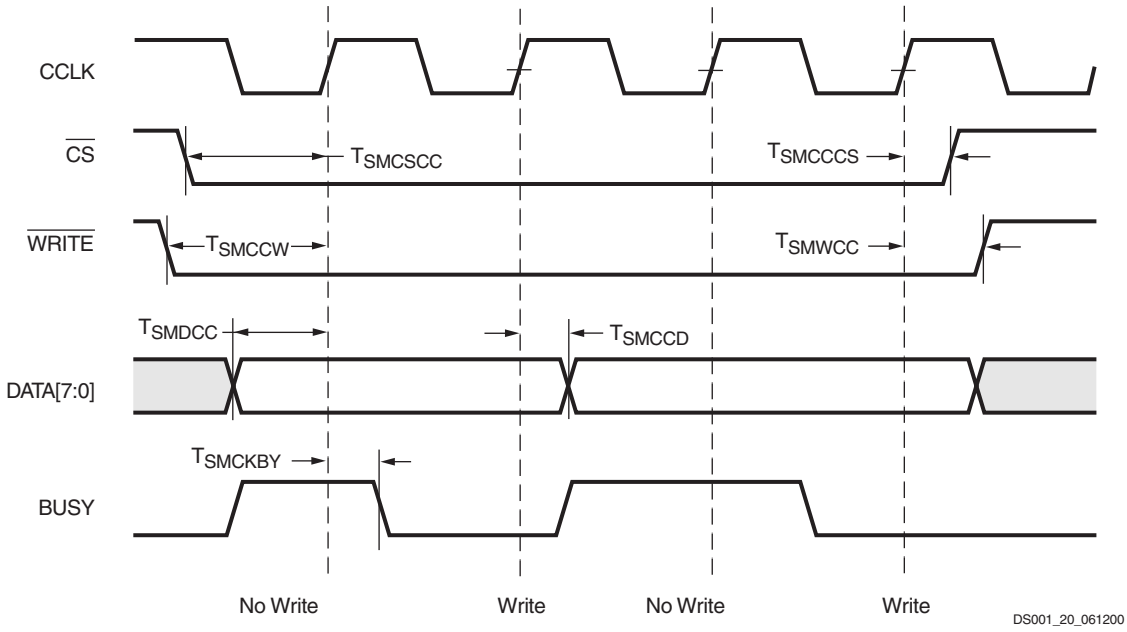
Symbol		Description	All Devices		Units
			Min	Max	
T_{DCC} / T_{CCD}	CCLK	DIN setup/hold	5 / 0	-	ns
T_{CCO}		DOUT	-	12	ns
T_{CCH}		High time	5	-	ns
T_{CCL}		Low time	5	-	ns
F_{CC}		Maximum frequency	-	66	MHz

Figure 3: **Slave Serial Mode Timing**



Symbol		Description	All Devices		Units
			Min	Max	
T_{DSCK} / T_{CKDS}	CCLK	DIN setup/hold	5 / 0	-	ns
T_{CCO}		DOUT	-	12	ns
F_{CC}		Frequency tolerance with respect to nominal	–30%	+45%	-

Figure 4: **Master Serial Mode Timing**



Symbol		Description	All Devices		Units
			Min	Max	
T_{SMDCC} / T_{SMCCD}	CCLK	D0-D7 setup/hold	5 / 1	-	ns
T_{SMCSCC} / T_{SMCCCS}		$\overline{CS}$ setup/hold	7 / 1	-	ns
T_{SMCCW} / T_{SMWCC}		$\overline{WRITE}$ setup/hold	7 / 1	-	ns
T_{SMCKBY}		BUSY propagation delay	-	12	ns
F_{CC}		Frequency	-	66	MHz
F_{CCNH}		Frequency with no handshake	-	50	MHz

Figure 5: **Slave Parallel (SelectMAP) Mode Write Timing**

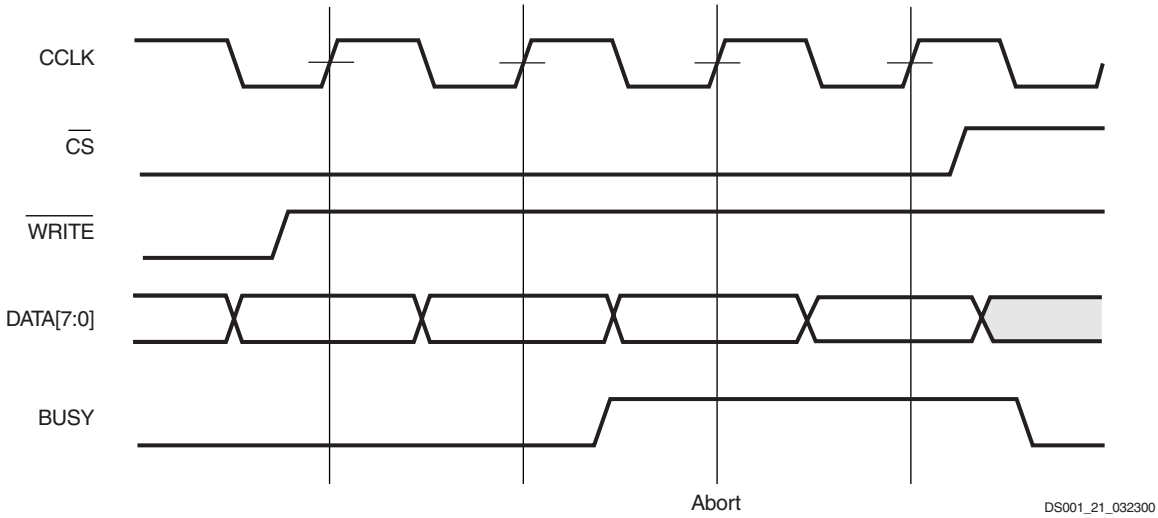


Figure 6: **Slave Parallel (SelectMAP) Mode Write Abort Waveforms**

Revision History

Version No.	Date	Description
1.0	11/15/01	Initial Xilinx release.
1.1	06/28/02	Added -7 speed grade and extended DLL specs to Industrial.
2.0	11/18/02	Added XC2S400E and XC2S600E. Added minimum specifications. Added reference to XAPP450 for Power-On Requirements. Removed Preliminary designation.
2.1	07/09/03	Added **ICCINTQ** typical values. Reduced **ICCPO** power-on current requirements. Relaxed **TCCPO** power-on ramp requirements. Added **IHSPO** to describe current in hot-swap applications. Updated **TPSFD / TPHFD** description to indicate use of delay element.

The Spartan-IIE Family Data Sheet

DS077-1, ***Spartan-IIE 1.8V FPGA Family: Introduction and Ordering Information*** (Module 1)

DS077-2, ***Spartan-IIE 1.8V FPGA Family: Functional Description*** (Module 2)

DS077-3, ***Spartan-IIE 1.8V FPGA Family: DC and Switching Characteristics*** (Module 3)

DS077-4, ***Spartan-IIE 1.8V FPGA Family: Pinout Tables*** (Module 4)